

SEMI M23-0623

SPECIFICATION FOR POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS

This Standard was technically approved by the Compound Semiconductor Materials Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on December 21, 2022. Available at www.semiviews.org and www.semi.org in June 2023; originally published in 1993; previously published February 2018.

NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§§ and §§§§) the symbols are used to reference more than one section or paragraph, respectively.

1 Purpose

1.1 This Specification covers the substrate requirements for monocrystalline high-purity indium phosphide wafers used in semiconductor and electronic device manufacturing. Dimensional and crystallographic orientation characteristics are the only standardized properties set forth below.

1.2 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed together with test methods suitable for determining their magnitude where such procedures are documented.

2 Scope

2.1 This Specification is directed specifically to indium phosphide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.2 The material is single crystal indium phosphide (InP) having a cubic zinc blend structure and the following properties:

Density	4.787 g/cm ³
Melting Point	1062°C
Dielectric Constant	12.4
Lattice Parameter	5.869 Å at 27°C
Energy Gap	1.351 eV at 27°C

2.3 For reference purposes SI (System International, commonly called metric) units shall be used.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M39 — Test Method for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility on Semi-Insulating GaAs Single Crystals

SEMI M59 — Terminology of Silicon Technology

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Test Method for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning (Withdrawn 0914)

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1393 — Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements with a Mercury Probe (Withdrawn 1105)

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T5 — Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers

3.2 *ANSI® Standards*¹

ANSI/ASQ Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM® Standards*²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, with Specified Precision, the Average for a Characteristic of a Lot or Process

ASTM F76 — Standard Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single-Crystal Semiconductors

3.4 *DIN Standards*³

DIN 50454-2 — Determination of the Dislocation Etch Pit Density in Monocrystals of III-V Compound Semiconductors – Part 2: Indium Phosphide.

DIN 50448 — Testing of Materials for Semiconductor Technology – Contactless Determination of the Electrical Resistivity of Semi-Insulation Semiconductor Slices using a Capacitive Probe

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Definitions*

NOTE 1: The selected terminology defined here has been adopted from SEMI M59.

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, <http://www.ansi.org>. ANSI trademark is owned by American National Standards Institute.

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

³ Deutsches Institut für Normung e.V., Am DIN-Platz, Burggrafenstrasse, D-10787 Berlin, Germany; Telephone: +49.30.2601.0, Fax: +49.30.2601.1231, <http://www.din.de>. DIN trademark is owned by Deutsches Institut für Normung e.V.

4.1.1 *bow (of a semiconductor wafer)* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer. Contrast flatness. Also refer to *warp*.

4.1.2 *dopant* — a chemical element, usually from the second, fourth, or sixth column of the periodic table for the case of III-V compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.3 *edge profile* — on wafers whose edges have been rounded by mechanical and/or chemical means, a description of the contour of the boundary of the wafer that joins the front and back surfaces.

4.1.4 *lot* — (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.5 *orthogonal misorientation* — in {100} wafers cut intentionally ‘off-orientation,’ the angle between the projection of the vector normal to the wafer surface onto the {100} plane and the projection on that plane of the nearest direction (refer to Figure 5).

4.1.6 *total indicator reading (TIR)* — on a wafer surface, the smallest perpendicular distance between two planes, both parallel with the reference plane, which enclose all points on the front surface of a wafer within the flatness quality area or the site, depending on which is specified.

4.1.7 *total thickness variation (TTV)* — of a semiconductor wafer, the difference between the maximum and minimum values of the thickness of the wafer.

4.1.8 *warp* — of a semiconductor wafer, the difference between the maximum and minimum distances of the median surface of a free, unclamped wafer from a reference plane, encountered during a scan pattern.

5 Ordering Information

5.1 Purchase orders for indium phosphide wafers furnished to this Specification shall include the following items:

5.1.1 Nominal diameter (refer to applicable SEMI Standard for Polished InP wafers),

5.1.2 Thickness (refer to applicable SEMI Standard for polished InP Wafers),

5.1.3 TTV, TIR, warp, and bow (determined by agreement between supplier and purchaser as to limits),

5.1.4 Surface orientation (refer to applicable SEMI Standard for polished InP wafers). There is only one option of flat location for 2 inch diameter polished monocrystalline InP wafers. The Dove-Tail option as illustrated in Figures 1 and Figure 3 are used for 2 inch diameter InP. There is a choice of dovetail or V-Groove options for 3 inch and 100 mm diameter wafers. These designations describe the shape of groove that can be etched perpendicular to the primary flat. The following are the options of wafer surface orientation:

- A. (100) $\pm 0.5^\circ$ as shown in Figures 1 and 2.
- B. (100) off 2° toward any of the nearest (110) planes. Examples shown in Figures 3 and 4.
- Direction of off-orientation can be designated by α angle (refer to Figure 5).
- Figure 5 illustrates orthogonal misorientation.

5.1.5 Lot acceptance procedures (refer to § 8),

5.1.6 Certification (refer to § 11), and

5.1.7 Packing and Marking (refer to § 12).

5.2 *Optional Criteria* — The following items may be specified optionally in addition to those listed above:

5.2.1 Crystal growth method,

5.2.2 Etch pit density (EPD) of crystal,

5.2.3 Crystal growth perfection,

- 5.2.4 Impurity type,
- 5.2.5 Surface condition of wafer,
- 5.2.6 Edge profile (refer to Figures 6 and 7),
- 5.2.7 Mobility,
- 5.2.8 Resistivity, and
- 5.2.9 Carrier concentration.

6 Materials and Manufacture

- 6.1 The material shall consist of wafers from ingots grown to the material defined in the purchase order or contract.

7 Physical and Electrical Requirements

- 7.1 The material shall conform to the crystallographic orientation details as specified in the applicable polished indium phosphide wafer standard.
- 7.2 The material shall conform to the details specified in the purchase order or contract as follows:
 - 7.2.1 Conduction Type,
 - 7.2.2 Dopant,
 - 7.2.3 Carrier Concentration,
 - 7.2.4 Resistivity,
 - 7.2.5 Etch Pit Density,
 - 7.2.6 Mobility,
 - 7.2.7 Surface Characteristics, and
 - 7.2.8 Growth Methods.

8 Sampling

- 8.1 Unless otherwise specified, ASTM E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQ Z1.4-1993. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4-1993 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

9 Test Methods

- 9.1 *Diameter* — Determined by SEMI MF2074.
- 9.2 *Thickness, Center Point* — Determined by SEMI MF533.
- 9.3 *Flat Length* — Determined by SEMI MF671.
- 9.4 *Flat Orientation* — Determined by etching method identified in the appropriate InP wafer standard.
- 9.5 *Total Thickness Variation* — Determined by SEMI MF533 or SEMI MF657.
- 9.6 *Surface Orientation* — Determined by SEMI MF26.
- 9.7 *Orthogonal Misorientation* — Determined by a method agreed upon between the supplier and purchaser.
- 9.8 *Surface Defects and Contamination* — Determined by SEMI MF154, SEMI MF523, or a method agreed upon between the supplier and purchaser.
- 9.9 *Mobility* — Determined by ASTM F76 or SEMI M39.
- 9.10 *Resistivity of Semi-insulating Wafers* — Determined by ASTM F76 or SEMI M39 or DIN 50448.