SEMI M23-1000
SPECIFICATION FOR POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the North American Compound Semiconductor Committee. Current edition approved by the North American Regional Standards Committee on August 28, 2000. Initially available at www.semi.org September 2000; to be published October 2000. Originally published in 1993; previously published September 1999.

NOTE: This document was entirely rewritten in 2000.

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1 Purpose

1.1 These specifications cover the substrate requirements for monocrystalline high-purity indium phosphide wafers used in semiconductor and electronic device manufacturing. Dimensional and crystallographic orientation characteristics are the only standardized properties set forth below.

1.2 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed together with test methods suitable for determining their magnitude where such procedures are documented.

2 Scope

2.1 These specifications are directed specifically to indium phosphide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.2 The material is Single Crystal Indium Phosphide (InP) having a cubic zinc blende structure and the following properties:

Density	4.787 g/cm^3
Melting Point	1062°C
Dielectric Constant	12.4
Lattice Parameter	5.869 A at 27°C
Energy Gap	1.351 eV at 27°C

2.3 For reference purposes SI (System International, commonly called metric) units shall be used.

2.4 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M39 — Test Method for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility on Semi-Insulating GaAs Single Crystals

3.2 *ASTM Standards*[1]

ASTM E 122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

ASTM F 26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

ASTM F 42 — Test Method for Conductivity Type of Extrinsic Semiconducting Materials

ASTM F 76 — Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single Crystal Semiconductors

ASTM F 84 — Test Methods for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

ASTM F 154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

ASTM F 523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

ASTM F 533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

ASTM F 534 — Test Method for Bow of Silicon Wafers

ASTM F 613 — Test Method for Measuring Diameter of Semiconductor Wafers

ASTM F 657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Non-Contact Scanning

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959 (All cited standards except for E 122 may be found in Volume 10.05 of the Annual Book of ASTM Standards; E 122 may be found in Volume 14.02.)

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ASTM F 671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

ASTM F673 — Test Method for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

ASTM F 928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

ASTM F1241 — Terminology of Silicon Technology

ASTM F 1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

ASTM F 1393 — Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements with a Mercury Probe

3.3 *Other Standard*

ANSI/ASQC[2] Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

DIN[3] Standard Test Method 50454-2 — Determination of the Dislocation Etch Pit Density in Monocrystals of III-V Compound Semiconductors - Part 2: Indium Phosphide.

4 Terminology

4.1 *Definitions*

NOTE 1: The selected terminology defined here has been adopted from ASTM Standard F 1241. Updates to this section are dependent on information exchange between ASTM and SEMI. Definitions are included for the benefit of the user, however, for a complete list, please refer to ASTM Standard F 1241.

4.1.1 *bow (of a semiconductor wafer)* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer. Contrast flatness. Also see warp.

4.1.2 *dopant* — a chemical element, usually from the second, fourth, or sixth column of the periodic table for the case of III-V compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.3 *edge profile* — on wafers whose edges have been rounded by mechanical and/or chemical means, a description of the contour of the boundary of the wafer that joins the front and back surfaces.

4.1.4 *lot* — for the purpose of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.5 *orthogonal misorientation* — in {100} wafers cut intentionally "off-orientation," the angle between the projection of the vector normal to the wafer surface onto the {100} plane and the projection on that plane of the nearest direction (see Figure 5).

4.1.6 *TIR* — on a wafer surface, the smallest perpendicular distance between two planes, both parallel with the reference plane, which enclose all points on the front surface of a wafer within the flatness quality area or the site, depending on which is specified.

4.1.7 *TTV, total thickness variation* — of a semiconductor wafer, the difference between the maximum and minimum values of the thickness of the wafer.

4.1.8 *warp* — of a semiconductor wafer, the difference between the maximum and minimum distances of the median surface of a free, unclamped wafer from a reference plane, encountered during a scan pattern.

5 Ordering Information

5.1 Purchase orders for indium phosphide wafers furnished to this specification shall include the following items:

5.1.1 Nominal diameter (see applicable SEMI Standard for Polished InP wafers),

5.1.2 Thickness (see applicable SEMI Standard for polished InP Wafers),

5.1.3 Total Thickness Variation, TIR, warp and bow (determined by agreement between supplier and purchaser as to limits),

5.1.4 Surface orientation (see applicable SEMI Standard for polished InP wafers). There is only one option of flat location for 2" diameter polished monocrystalline InP wafers. The Dove-Tail option as illustrated in Figures 1 and 3 is used for 2" diameter InP. There is a choice of dovetail or V-Groove options

2 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

3 Deutsches Institut fur Normung e.v., available from Beuth Verlag, Burggrafenstrasse 6, D-10787 Berlin, Germany

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for 3" and 100mm diameter wafers. These designations describe the shape of groove that can be etched perpendicular to the primary flat. The following are the options of wafer surface orientation:

A. (100) ± 0.5° as shown in Figures 1 and 2

B. (100) off 2° toward any of the nearest (110) planes. Examples shown in Figures 3 and 4.

Direction of off-orientation can be designated by α angle. (See Figure 5)

Figure 5 illustrates orthogonal misorientation.

5.1.5 Lot acceptance procedures (see Section 8),

5.1.6 Certification (see Section 11),

5.1.7 Packing and Marking (see Section 12).

5.2 *Optional Criteria* — The following items may be specified optionally in addition to those listed above:

5.2.1 Crystal growth method,

5.2.2 Etch Pit Density (EPD) of Crystal,

5.2.3 Crystal Growth Perfection,

5.2.4 Impurity Type,

5.2.5 Surface Condition of Wafer,

5.2.6 Edge Profile (see Figures 6 and 7),

5.2.7 Mobility,

5.2.8 Resistivity, and

5.2.9 Carrier Concentration.

6 Materials and Manufacture

6.1 The material shall consist of wafers from ingots grown to the material defined in the purchase order or contract.

7 Physical and Electrical Requirements

7.1 The material shall conform to the crystallographic orientation details as specified in the applicable polished indium phosphide wafer standard.

7.2 The material shall conform to the details specified in the purchase order or contract as follows:

7.2.1 Conduction Type,

7.2.2 Dopant,

7.2.3 Carrier Concentration,

7.2.4 Resistivity,

7.2.5 Etch Pit Density,

7.2.6 Mobility,

7.2.7 Surface Characteristics, and

7.2.8 Growth Methods.

8 Sampling

8.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4-1993. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4-1993 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

9 Test Methods[4]

9.1 *Diameter* — Determined by ASTM Test Method F 613.

9.2 *Thickness, Center Point* — Determined by ASTM Test Method F 533.

9.3 *Flat Length* — Determined by ASTM Test Method F 671.

9.4 *Flat Orientation*[5] — Determined by etching method identified in the appropriate InP wafer standard.

9.5 *Total Thickness Variation* — Determined by ASTM Test Method F 533 or F 657.

9.6 *Surface Orientation* — Determined by ASTM Test Method F 26.

9.7 *Orthogonal Misorientation* — Determined by a method agreed upon between the supplier and purchaser.

9.8 *Surface Defects and Contamination* — Determined by ASTM Test Methods F154, F523 or a method agreed upon between the supplier and purchaser.

9.9 *Mobility and Resistivity* — Determined by ASTM Test Methods F 76 or SEMI M39.

4 InP wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as a micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must, therefore, be used in the selection and execution of measurement methods.

5 Relating to the etchant used for identifying V-groove and/or dovetail direction, see reference: "HBr-K_2 Cr_2O_7 – H_2O etching system for indium phosphide" J.L. Weyher, et al. Materials Science and Engineering B28 (1994) 488-492.

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9.10 *Crystal Perfection* — Determined by a method agreed upon between the supplier and purchaser.

9.11 *Edge Contouring* — Determined by ASTM Test Method F 928.

9.12 *Conductivity or Resistivity of Doped Wafers* — Determined by ASTM Test Method F76 or F84 or F673.

9.13 *Bow* — Determined by ASTM Test Method F534 or a method agreed upon between the supplier and purchaser.

9.14 *Etch Pit Density* (*EPD*) — Determined by DIN Standard Test Method 50454-2

9.15 *Carrier concentration* — Determined by ASTM Test Method F76 or F1392 or F1393 or Electrochemical CV[6].

9.16 *Conductivity Type* — Determined by ASTM Test Method F42 or F76.

10 Standard Defect Limits

10.1 Limits are determined by an agreement between supplier and purchaser.

11 Certification

11.1 A manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results. A certification shall be furnished at the time of shipment, upon the request of the purchaser in the contract or order.

12 Packing and Marking

12.1 Special packing and marking requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed with the best industry practices to provide ample protection against damage during shipment.

12.2 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision that the wafers will be stored prior to further processing. Identification shall include lot number and wafer number. Per the agreement between the supplier and purchaser, the following must be accessible from the lot and wafer numbers: nominal diameter, conductive dopant, orientation, resistivity, and EPD. Such information shall be retained on file at the manufacturer's facility for at least one month or as negotiated between vendor and user after that particular lot has been accepted by the purchaser.

13 Related Documents

"HBr-$K_2Cr_2O_7$ – H_2O etching system for indium phosphide" J.L. Weyher, et al. Materials Science and Engineering B28 (1994) 488-492.

6 NOTE: Electrochemical CV test method has not been completed but is in the process of being developed by the industry.

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