

SEMI M24-0307

SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON PREMIUM WAFERS

This standard was technically approved by the global Silicon Wafer Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on November 21, 2006. It was available at www.semi.org in February 2007 and on CD-ROM in March 2007. Originally published in 1994; previously published November 2005.

1 Purpose

1.1 This document specifies requirements for virgin silicon premium wafers with nominal diameter from 150–300 mm used for particle counting, metal contamination monitoring, and measuring pattern resolution in the photolithography process in semiconductor manufacturing. The premium wafer has tighter specification values in some specific items for the specific usage, and looser or equal specification values in other items than a prime wafer has.

2 Scope

2.1 This specification classifies premium wafers according to surface condition and dimensional tolerances. Premium wafer classifications are summarized in Table 1.

2.2 Specification values are determined by the use for which the wafers are intended.

2.3 This specification provides premium wafers that can be used to test and evaluate leading edge device process.

2.4 For referee purposes, SI (System International) units shall be used.

2.5 The complete EDI Code List for items in the Order Form appropriate to silicon wafers, including polished wafers, can be found in SEMI M18.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers

SEMI M45 — Provisional Specification for 300 mm Wafer Shipping System

SEMI M59 — Terminology for Silicon Technology

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 ANSI Standards¹

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/EIA 556-B — Outer Shipping Container Standard

3.3 ASTM Standard²

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

1 American National Standards Institute, Headquarters: 1819 L Street, NW, Washington, DC 20036, USA. Telephone: 202.293.8020; Fax: 202.293.9287, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023; Website: <http://www.ansi.org>

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; Website: <http://www.astm.org>

3.4 ISO Standard³

ISO 14644-1 — Cleanrooms and associated controlled environments — Part 1: Classification of air cleanliness

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Most general terms, acronyms, and symbols relating to silicon technology are defined in SEMI M59.

5 Ordering Information

5.1 Purchase orders for silicon premium wafers furnished to this specification shall include the appropriate order entry information from Table 1, Polished Wafer Specification Format for Order Entry, in SEMI M1. All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included:

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions
- 2-6.3 Primary Flat/Notch Orientation
- 2-6.6 Edge Profile
- 2-6.7 Thickness

Other items shall be included as agreed between supplier and customer.

5.2 In addition, the purchase order must indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

5.3 The parameter values provided in Tables 2, 3, and 4 may be used to identify appropriate values in the specification without selecting a value for each line. At the time, the appropriate specification group listed in Table 1 is used.

5.4 For items in Tables 2, 3, and 4 that contain alternative specifications, the desired specification must be contained in the purchase order unless the supplier has the option which specification to use. Note that items that specify 'SEMI M1' generally need to be further specified because SEMI M1 frequently has several values for such items.

Table 1 Wafer Classifications

<i>Classification</i>	<i>Application</i>
Particle Counting	Particle counting
Furnace and Thermal Process	Metal contamination monitoring
Lithography and Patterning	Measurement of pattern resolution in photolithography

5.5 The following items must also be included in the purchase order:

5.5.1 Lot acceptance procedures.

5.5.2 Certification (if required).

5.5.3 Packing and shipping container labeling requirements.

³ International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembe, Case postale 56, CH-1211 Geneva 20, Switzerland.
Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; Website: <http://www.iso.ch>

6 Requirements

6.1 Tables 2, 3, and 4 provide Specifications for Polished Monocrystalline Silicon Premium Wafers for 180, 130, and 90 nm Design Rule Usages. A parameter not listed in these tables need not be specified. The specification for 250 nm Design Rule Usage was deleted in SEMI M24 at publication in November 2003, the original table can be referred to in SEMI M24 1999–2001 versions.

6.2 It is also essential to specify appropriate test methods in each case. Defaults for test method selection are given in § 8.

NOTE 1: The line items with numbers beginning with “2-” are listed in Part 2 of the Silicon Wafer Specification Format for Order Entry, SEMI M1, Table 1.

7 Sampling

7.1 Unless otherwise specified, ASTM Practice E 122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the customer.

8 Test Methods

8.1 Measurements shall be made or certifiable to one of the SEMI, ASTM, JEITA, JIS, or DIN standard test methods for the item as selected from the Silicon Wafer Specification Format for Order Entry, Part 2, located in Table 1 of SEMI M1, and specified in the purchase order.

8.2 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

8.3 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method shall be a method in common usage for the region of the purchaser of the wafer.

8.4 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

8.5 Information about the various test methods cited is provided in Related Information 2 of SEMI M1 together with information about some additional test methods no longer in wide use throughout the industry.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer’s or supplier’s certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 In the interest of controlling inspection costs, the supplier and the customer may agree that the material shall be certified as “capable of meeting” certain requirements. In this context, “capable of meeting” shall signify that the supplier is not required to perform the appropriate tests in § 8. However, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Product Labeling

10.1 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer’s facility for at least one month after that particular lot has been accepted by the customer.

10.2 Alternatively, if agreed upon between supplier and customer, one of the box labeling schemes in SEMI T3 shall be used and the information listed in ¶ 10.1 that is not included on the label shall be retained in the supplier’s data base for at least one month after that particular lot has been accepted by the customer.

10.3 Wafers of 300 mm diameter shall be shipped in packages labeled in accordance with SEMI M45.

11 Packing and Shipping Container Labeling

11.1 Special packing requirements shall be subject to agreement between the supplier and customer. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices, to provide ample protection against damage during shipment.

11.2 Wafers of 300 mm diameter shall be shipped in accordance with SEMI M45.

11.3 Unless otherwise indicated in the purchase order, all outside wafer shipping containers shall be labeled in accordance with ANSI/EIA 556-B.

Table 2 Specification for Polished Monocrystalline Silicon Premium Wafers for 180 nm Design Rule Usage

ITEMS	Particle Counting	Furnace & Thermal Process	Lithography & Patterning
2-1 GENERAL CHARACTERISTICS			
2-1.1 Growth Method	Cz or MCz	Cz or MCz	Cz or MCz
2-1.3 Crystal Orientation	(100) ± 1°	(100) ± 1°	(100) ± 1°
2-1.4 Conductivity Type	n or p	n or p	n or p
2-1.5 Dopant	P or B	P or B	P or B
2-1.6 Nominal Edge Exclusion ^{#1}	300 mm: 2 mm 200 mm: 3 mm	300 mm: 2 mm 200 mm: 3 mm	300 mm: 2 mm 200 mm: 3 mm
2-1.8 Wafer Surface Orientation	-	-	-
2-2 ELECTRICAL CHARACTERISTICS			
2-2.1 Resistivity, Measured at	NS	≥1 Ω-cm Center Point ^{#4}	NS
2-2.2 Radial Resistivity Variation (RRG)	NS	NS	
2-2.4 Minority Carrier Lifetime	NS	≥325 μs ^{#4}	
2-3 CHEMICAL CHARACTERISTICS			
2-3.1 Oxygen Concentration: Spec. Range of Center Point: Target	NS	≤1.2 × 10 ¹⁸ /cm ³ IOC-88	NS
2-3.1 Oxygen Concentration: Tolerance Around Center Point: Target		≤10%	
2-3.2 Radial Oxygen Variation		NS	
2-3.3 Carbon Concentration		≤0.2 ppma	
2-3.5 Total Bulk Iron Concentration		≤5 × 10 ¹⁰ /cm ³ ^{#4}	
2-4 STRUCTURAL CHARACTERISTICS			
2-4.1 Dislocation Etch Pit Density	NS	≤500/cm ²	NS
2-4.2 Slip		None	
2-4.3 Lineage		None	
2-4.4 Twin		None	
2-4.5 Swirl		None	
2-4.6 Shallow Pits		None	
2-4.7 Oxidation Induced Stacking Faults (OSF)	NS	Supplier/Customer	NS
2-4.8 Oxide Precipitates (BMD)		Supplier/Customer	
2-4.9 Interstitial Oxygen Reduction (Δ Oi)		Supplier/Customer	
2-5 WAFER PREPARATION CHARACTERISTICS			
2-5.1 Wafer ID Marking ^{#2}	Optional	Optional	Optional