SEMI M24-1101
SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON PREMIUM WAFERS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on August 3, 2001. Initially available at www.semi.org September 2001; published November 2001. Originally published in 1994; previously published March 2001.

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1 Purpose

1.1 This document specifies requirements for virgin silicon premium wafers with nominal diameter from 150 mm to 300 mm used for particle counting, metal contamination monitoring, and measuring pattern resolution in the photolithography process in semiconductor manufacturing. The premium wafer has tighter specification values in some specific items for the specific usage, and looser or equal specification values in other items than a prime wafer has.

2 Scope

2.1 This specification classifies premium wafers according to surface condition and dimensional tolerances. Premium wafer classifications are summarized in Table 1.

2.2 Specification values are determined by the use for which the wafers are intended.

2.3 This specification provides premium wafers that can be used to test and evaluate leading edge device process.

2.4 For referee purposes, SI (System International) units shall be used.

2.5 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M20 — Specification for Establishing a Wafer Coordinate System

SEMI M25 — Specification for Silicon Wafers for Calibration of Light Point Defect Wafer Inspection Systems with Respect to the Diameter of Polystyrene Latex Spheres

3.2 *ANSI Standard*[1]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standards*[2]

D 523 — Standard Test Method for Specular Gloss

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

F 26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F 42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

F 47 — Standard Test Method for Crystallographic Perfection of Silicon by Preferential Etch Techniques

F 84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Probe Array

F 154 — Standard Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F 391 — Standard Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

F 416 — Standard Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers

F 523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surface

F 533 — Standard Test Method for Thickness and Thickness of Variation of Silicon Wafers

F 534 — Standard Test Method for Bow of Silicon Wafers

F 613 — Standard Test Method for Measuring Diameter of Semiconductor Wafers

1 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959

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F 657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

F 671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Material

F 673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

F 847 — Standard Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

F 928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

F 978 — Standard Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

F 1049 — Standard Practice for Shallow Pit Detection on Silicon Wafers

F 1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

F 1188 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

F 1239 — Standard Test Methods for Oxygen Precipitation Characterization of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

F 1241 — Standard Terminology of Silicon Technology

F 1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

F 1391 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

F 1451 — Standard Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

F 1526 — Standard Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy

F 1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

F 1535 — Standard Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

F 1617 — Standard Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and EPI Substrates by Secondary Ion Mass Spectroscopy

F 1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle

F 1620 — Standard Practice for Calibrating a Scanning Surface Inspection System Using Monodisperse Polystyrene Latex Spheres Deposited on Polished or Epitaxial Surfaces

F 1621 — Standard Practice for Determining Positional Accuracy Capabilities of a Scanning Surface Inspection System

3.4 *DIN Standards*[3]

50431 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Colinear Four-Probe Array

50432 — Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe

50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

50433/2 — Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure

50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back Scattering

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

50435 — Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe

50438/1 — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen

50438/2 — Determination of Impurity Content in Silicon by Infrared Absorption: Carbon

50438/3 — Determination of Impurity Content in Silicon by Infrared Absorption: Boron and Phosphorus

50441/1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

3 Deutsches Institut für Normung e.v., available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany

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50441/2 — Determination of the Geometric Dimensions of Semiconductor Slices: Testing of Edge Rounding

50441/4 — Determination of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices

50443/1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-Ray Topography: Silicon

50445 — Contactless Determination of the Electrical Resistivity of Semiconductor Wafers with the Eddy Current Method

3.5 *JEITA Standards*[4]

JEIDA 18 — Determining the Orientation of a Semiconductor Silicon Single Crystal

JEIDA 27 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surface

JEIDA 43 — Terminology of Silicon Wafer Flatness

JEIDA 53 — Test Method for Recombination Lifetime in Silicon Wafers by Measurement of Photoconductivity Decay by Microwave Reflectance

JEIDA 56 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

JEIDA 61 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

3.6 *JIS Standards*[5]

H 0602 — Testing Method of Resistivity for Silicon Crystals and Silicon Wafers with Four-Point Probe

H 0607 — Testing Methods for Conductivity Type of Semiconductor Materials

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0611 — Methods of Measurement of Thickness, Taper, and Bow of Silicon Wafers

H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

Z8741 — Method of Measurement for Specular Glossiness

4 Japan Electronics and Information Technology Industries Association, 3rd Floor Mitsui Kaijo Bldg. Annex 11, Kanda Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan

5 Japanese Standard Association 1-24, Akasaka 4 Chome, Minato-ku, Tokyo 107-0000, Japan

NOTE 1: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions of terms related to silicon wafer technology are given in ASTM Terminology F 1241.

4.2 Definitions for some additional terms are given in SEMI M1.

4.3 The following definitions apply in the context of this specification:

4.3.1 *furnace and thermal processes* — wafers intended for use in evaluating metal contamination in thermal process.

4.3.2 *hand scribe mark* — any marking, usually on the back surface of a wafer, scratched manually into the silicon surface, as with a diamond-tipped scribe, for purposes of wafer identification.

4.3.3 *lithography and patterning* — wafers intended for use in evaluating pattern resolution.

4.3.4 *particle counting* — wafers intended for use in evaluating the particulate contamination added by a process tool. LLSs (Localized Light Scatterers) include particles and COP (Crystal Originated Pits).

4.3.5 *premium wafer* — a silicon wafer suitable for particle counting, metal contamination monitoring, and measuring pattern resolution in the photolithography process. The premium wafer has tighter specification values in some specific items for the specific usage, and looser or equal specification values for other items than a prime wafer has.

5 Ordering Information

5.1 Purchase orders for silicon premium wafers furnished to this specification shall include the items from the appropriate specification groups listed in Table 1.

Table 1 Wafer Classifications

Classification	*Application*
Particle Counting	Particle counting
Furnace and Thermal Process	Metal contamination monitoring
Lithography and Patterning	Measurement of pattern resolution in photolithography

5.2 Items which may be specified when ordering silicon wafers are listed in attached specification tables. Not all of these items are required for ordering premium wafers.

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6 Dimensions and Permissible Variations

6.1 The material shall conform to the dimensions and dimensional tolerances in attached specification tables.

7 Materials and Manufacture

7.1 The material shall consist of wafers from crystals grown by the process specified in the purchase order or contract.

8 Physical Requirements

8.1 The material shall conform to the details specified in the purchase order.

9 Sampling

9.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) and lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

10 Test Methods

10.1 Table 1 of SEMI M18 contains a complete listing of ASTM, DIN, and JEIDA/JIS test methods that may apply to the testing of specified premium silicon wafers. These attributes are listed in the order they are found in the specification (which corresponds to the order in SEMI M18).

10.2 *Conductivity Type* — Use any of the methods in ASTM Test Methods F 42, JIS H 0607, or DIN 50432 for confirming the conductivity type of silicon wafers covered by this specification.

10.3 *Dopant* — Confirm the dopant of high resistivity silicon by the photoluminescence method of ASTM Test Method F 1389 or by the low-temperature infrared method of ASTM Test Method F 1630 or DIN 50438/3.

10.4 *Resistivity* — Determine the electrical resistivity of the wafer in accordance with ASTM Test Method F 673 or DIN 50445 (eddy current), or ASTM Test Method F 84, JIS H 0602, or DIN 50431 (four point probe) using a suitable fixture to hold the wafer.

10.5 *Carrier Recombination Lifetime* — Determine in accordance with F 1535 or JEIDA 53.

10.6 *Oxygen Content* — Determine the interstitial oxygen content of wafers with resistivity greater than a few ohm-cm by infrared absorption. ASTM Test Method F 1188 is the method that was used in analyzing the results of the international round robin experiment that established the IOC-88 conversion coefficient. DIN 50438/1 provides improved procedures of correcting for back surface roughness and multiple internal reflections. ASTM Test Method F 1619, based on work carried out in JEIDA (JEIDA 61) and SEMI Japan, is an alternative procedure for significantly reducing errors associated with these two phenomena.

10.7 *Carbon Content* — For all but very heavily doped epitaxial substrates, establish the carbon content in accordance with ASTM Test Method F 1391, JEIDA 56, or DIN 50438/2.

10.8 *Total Bulk Iron* — No standardized test method exists for direct determination of total bulk iron content in silicon. ASTM Test Method F 978 can be used for direct determination of the electrically active iron. Extensions of the surface photovoltage method (ASTM Test Method F 391) and of the microwave lifetime method (ASTM Test Method F 1535) have been reported in the literature to provide information on total bulk iron content of boron-doped silicon; both these extensions are based on the iron-boron pairing process.

10.9 *Structural Characteristics* — When feasible observe crystal defects such as dislocation etch pits, slip, lineage, twins, etc., in accordance with ASTM Test Method F 47, JIS H 0609, or DIN 50434. These methods are destructive, and with the exception of JIS H 0609 are based on chromium-containing etchants. Some structural defects, especially slip, can be determined nondestructively by means of X-ray topographic analysis in accordance with DIN 50443/1. Swirl and oxidation induced stacking faults (OSFs) are best observed after heat treatment such as those specified in ASTM Practice F 416. However, the heat cycles in this practice were developed for 100 mm wafers and are not suitable for 300 mm wafers. Accordingly, thermal cycles used shall be agreed upon between supplier and purchaser. For observation of OSFs, a 2-hour heat treatment at 1100°C in steam is recommended. Observe shallow pits in accordance with ASTM Practice F 1049.

10.10 *Diameter* — Diameter may be determined in accordance with ASTM Test Method F 613 or DIN 50441/4. Because notched wafers do not have flats, it is not necessary to make the measurements along the particular diameters identified in ASTM Test Method F 613; rather it is suggested that measurements be made along the diameter perpendicular to the <100> orientation fiducial axis (0° in the coordinate system specified in SEMI M20), the diameter 120° counter-clockwise, and the diameter 240° counterclockwise. However, a more precise method of determining the

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diameter is to find the circle that best fits the circumference of the wafer by a least squares method; the diameter of the wafer is twice the radius of this circle.

10.11 *Flat Orientation* — Determine in accordance with ASTM Test Method F 847.

10.12 *Flat Length* — Determine in accordance with ASTM Test Method F 671.

10.12.1 If flat diameter is specified instead of flat length, determine in accordance with Section 5.2.1 of DIN 50441/4 or by a dial gauge method (see NOTE 8) as agreed upon between supplier and purchaser.

10.13 *Notch Dimension* — Determine the depth and angle of the fiducial notch in accordance with ASTM Test Method F 1152 with the use of a wafer holding fixture appropriate for silicon wafers.

10.14 *Notch Orientation* — No test method for verifying the crystal axis of the orientation fiducial axis of notched wafers has yet been standardized. Accordingly, test procedures for making this determination shall be agreed upon between supplier and purchaser. A starting point may be an extension of ASTM Test Method F 847 with fixturing appropriate to notched wafers.

10.15 *Edge Profile Shape* — Determine the suitability of the edge profile in accordance with ASTM Test Method F 928 or DIN 50441/2.

10.16 *Edge Surface Finish* — Establish the surface finish of the edge region of the wafer by a method agreed upon between supplier and purchaser.

10.17 *Thickness, Center Point* — Determine thickness, center point may in accordance with ASTM Test Method F 533, JIS H 0611, or DIN 50441/1; special jigs or fixtures may be needed to allow the probe to reach the center point of the wafer.

10.18 *Total Thickness Variation* — Determine in accordance with ASTM Test Method F 533, ASTM Test Method F 657, DIN 50441/1, and JIS H 0611.

NOTE 2: ASTM Test Method F 533, DIN 50441/1, and JIS H 0611 are all 5-point methods, while Test Method F 657 involves a continuous scan pattern. JIS H 0611 differs from ASTM Test Method F 533 and DIN 50441/1 in that the measurements in JIS H 0611 are taken at the center and at 5 mm from the edge on diameters parallel and perpendicular to the major flat, while the measurements in the latter two test methods are taken at the center and at the same radial distance (R nominal - 6 mm) on diameters 30 degrees and 120 degrees counterclockwise from the bisector to the primary flat or notch (with the wafer facing front surface up).

10.19 *Surface Orientation* — Determine the crystallographic orientation of the wafer surface in accordance with ASTM test methods F 26, JEIDA Method 18, or DIN 50433 using a suitable fixture to hold wafer.

10.20 *Bow and Warp* — Determine bow in accordance with ASTM Test Method F 534 and warp in accordance with ASTM Test Method F 1390 or Test Method F 657.

NOTE 3: ASTM has standardized two methods for measuring warp. ASTM Test Method F 1390 is an automated, non-contact method which provides for correction of the wafer deflection due to gravitational effects. The scan pattern covers the entire fixed quality area. ASTM Test Method F 657 is a manual, non-contact method which has a continuous, prescribed scan pattern which covers only a portion of the wafer surface. There is no provision for correction of the wafer deflection due to gravitational effects. As noted in Appendix 2, different reference planes are used for the two methods. Because Test Method F 657 employs a back surface reference plane, the measured warp may include contributions from thickness variation of the wafer. Test Method F 1390 employs a median surface reference plane and is not susceptible to interferences from thickness variations. In general, Test Method F 1390 is preferred, especially for wafers 150 mm in diameter and larger, although ASTM Test Method F 1530 may also be used for this determination.

10.21 *Sori* — If sori is specified in lieu of bow or warp or both, determine by a method agreed upon between the supplier and the purchaser.

NOTE 4: Because sori is a property of the top surface of an unclamped wafer, it may be measured on many types of flatness measuring instruments. ASTM Test Method F 1451 may, in principle, be used for determination of sori.

10.22 *Flatness* — Determine by a method agreed upon between the supplier and the purchaser. It is recommended that site flatness is determined in accordance with ASTM Test Method F 1530 using a site-by-site front surface reference (indicated by the acronym SFQR in the Flatness Decision tree (see SEMI M1, Figure A1-1)). The percent usable area (PUA) shall be calculated as the percentage of the total number of full sites within the FQA that meet the specification.

10.23 *Surface Metal Contamination* — Determine surface metal contamination by a method agreed upon between supplier and purchaser; ASTM Test Method F 1617 is suitable for sodium and aluminum, and ASTM Test Method F 1526 is suitable for chromium, iron, nickel, copper, and zinc at the specified levels. Other, more sensitive methods may also be utilized by agreement between supplier and purchaser.

10.24 *Back Surface Gloss* — Determine test method in accordance with ASTM D523 or JIS Z8741 using a 60 degree of incidence and referencing the zero to a mirror polished wafer front surface instead of reference gloss surface as described in these feat method.

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11 Surface Defect Criteria

11.1 Front surface defect criteria are shown in Item 8 in attached specification tables.

11.2 *Minimal Conditions or Dimensions* — The minimal conditions or dimenions for defects stated below shall be used for determining wafer acceptability. Anomalies smaller than these limits shall not be considered defects.

11.2.1 *area contamination* — Any foreign matter on the surface in localized areas which is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains, water spots, etc.

11.2.2 *crack* — Any anomaly conforming to the definition and greater than 0.25 mm (0.010 inch) in total length.

11.2.3 *crow's foot* — Any anomaly conforming to the definition and greater than 0.25 mm (0.010 inch) in total length.

11.2.4 *dimple* — Any smooth surface depression greater than 3 mm in diameter.

11.2.5 *edge chip and indent* — Any edge anomaly, including saw exit marks, conforming to the definition and greater than 0.25 mm (0.010 inch) in radial depth and peripheral length.

11.2.6 *hand scribe mark* — Any mark such as that caused by a diamond scribe that is visible under diffuse illumination.

11.2.7 *haze* — Haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the polished wafer surface. (Under some conditions, contamination may appear as haze.)

11.2.8 *orange peel* — Any roughened surface conforming to the definition that is observable under diffuse illumination.

11.2.9 *particulate contamination* — Distinct particles, resting on the surface, which are revealed under collineated light as bright points.

11.2.10 *pit* — Any individually distinguishable non-removable surface anomaly conforming to the definition and visible when viewed under high intensity illumination.

11.2.11 *saw marks* — Any surface irregularities conforming to the definition that are observable under diffuse illumination.

11.2.12 *scratch* — Any anomaly conforming to the definition and having a length-to-width ratio greater than 5:1.

11.2.13 *slip* — Any pattern of short ridges aligned along <111> directions and visible under diffuse illumination.

11.2.14 *striations* — Any helical features conforming to the definition and visible under diffuse illumination.

11.3 Back surface defect criteria are specified in attached specification tables.

12 Certification

12.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

12.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 10. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

13 Packing and Marking

13.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices, to provide ample protection against damage during shipment.

13.2 The wafers supplied under this specification shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include, as a minimum, wafer classification, nominal diameter, surface orientation, growth method, lot number, and origin. In addition, identification of premium wafers shall include conductivity type and resistivity range of the lot. The lot number, either (1) assigned by the original manufacturer of the wafer, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the vendor's facility for at least one month after that particular lot has been accepted by the purchaser.

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