

SEMI M28-0997 (Withdrawn 1000) SPECIFICATION FOR DEVELOPMENTAL 300 mm DIAMETER POLISHED SINGLE CRYSTAL SILICON WAFERS

This document was balloted and approved for withdrawal in 2000.

NOTE: This entire document was revised in 1997.

1 Purpose

1.1 The developmental wafers covered by this specification are intended for use in research on and development of process and metrology equipment and fabrication processes required to manufacture high-density integrated circuits on 300 mm diameter single crystal silicon wafers. They can also be used to establish the techniques and metrology necessary to support a dimensional specification for 300 mm diameter circuit-quality (prime) wafers.

2 Scope

2.1 This specification covers dimensional and crystallographic orientation requirements for 300 mm diameter polished single crystal silicon wafers that fill a short term need for developmental wafers; it is intended to withdraw this document in favor of a dimensional specification and technology specific guidelines for circuit-quality wafers during 1998.

2.2 A complete purchase specification requires that additional physical properties be specified along with test methods for determining their magnitude (see Section 5).

2.3 Wafers meeting the basic specification requirements herein are suitable for use as “mechanical” wafers for equipment set-up and robotic handling applications.

2.4 This specification also contains guides to assist equipment manufacturers and others to specify wafers for use in developing selected process equipment and unit processes (see Appendix 1).

2.5 For referee purposes, SI (System International, commonly called metric) units shall be used.

3 Referenced Documents

3.1 SEMI Standards

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M20 — Specification for a Establishing a Wafer Coordinate System

3.2 ASTM Standards¹

D 523 — Test Method for Specular Gloss²

E 122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process³

F 26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F 42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

F 47 — Test Method for Crystallographic Perfection of Silicon by Preferential Etch Techniques

F 84 — Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

F 391 — Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

F 416 — Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers

F 523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

F 533 — Test Method for Thickness and Thickness Variation of Silicon Slices

F 613 — Test Method for Measuring Diameter of Semiconductor Wafers

F 657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Slices and Wafers by Noncontact Scanning

F 673 — Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

F 847 — Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

F 928 — Test Methods for Edge Contour of Silicon Wafers

¹ Except for ASTM D 523 and ASTM E 122, Annual Book of ASTM Standards, Volume 10.05, published annually by the American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959.

² loc. cit., Volume 6.01

³ loc. cit., Volume 14.02

F 951 — Test Method for Determination of Radial Interstitial Oxygen Variation

F 978 — Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

F 1049 — Practice for Shallow Pit Detection on Silicon Wafers

F 1152 — Test Method for Dimensions of Notches on Silicon Wafers

F 1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

F 1241 — Terminology of Silicon Technology

F 1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry

F 1389 — Test Methods for Photoluminescence Analysis of Single Crystal Silicon for III-V Impurities

F 1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

F 1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

F 1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

F 1526 — Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence Spectroscopy

F 1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

F 1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

F 1617 — Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

F 1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle

F 1620 — Practice for Calibrating a Scanning Surface Inspection System Using Monodisperse Polystyrene Latex Spheres Deposited on Polished or Epitaxial Surfaces

F 1621 — Practice for Determining Positional Accuracy Capabilities of a Scanning Surface Inspection System

F 1630 — Test Method for Low Temperature FT-IR Analysis of Single Crystal Silicon for III-V Impurities

3.3 DIN Standards⁴

50431 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Collinear Probe Array

50432 — Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot Probe

50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

50433/2 — Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure

50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back-Scattering

50434 — Determination of the Crystal Perfection of Monocrystalline Silicon by Preferential Etch Techniques on {111}- and {100}-Surfaces

50438/1 — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen

50438/2 — Determination of Impurity Content in Silicon by Infrared Absorption: Carbon

50438/3 — Determination of Impurity Content in Silicon by Infrared Absorption: Boron and Phosphorus

50441/1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

50441/2 — Determination of the Geometric Dimensions of Semiconductor Slices; Testing of Edge Rounding

50441/4 — Determination of the Geometric Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices

50443/1 — Recognition of Defects and Inhomogeneities in Semiconductor Single Crystals by X-Ray Topography: Silicon

50445 — Contactless Determination of the Electrical Resistivity of Semiconductor Wafers with the Eddy Current Method

⁴ Deutsches Institut für Normung, e.v.; German editions available from Beuth Verlag GmbH, Burggrafenstraße 4-10, D-1000 Berlin 30, Germany. English translations included in Reference 1.

3.4 JIS Standards⁵

H 0602 — Testing Method of Resistivity for Silicon

H 0607 — Test Methods for Conductivity Type of Semiconductor Materials

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0611 — Methods of Measurement of Thickness, Taper and Bow for Silicon Wafers

H 0612 — Testing Method of Resistivity for Single Crystal Silicon Wafers (with Four Point Probe)

H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

Z 8741 — Method of Measurement for Specular Glossiness

3.5 JEIDA Standard⁶

18 — Determining the Orientation of a Semiconductor Silicon Single Crystal

3.6 ANSI Standard⁷

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

4 Terminology

4.1 Many of the terms used in this specification are defined in SEMI M1.

4.2 Additional terms are defined in ASTM Terminology F 1241.

5 Wafer Ordering Information

5.1 Purchase orders for silicon wafers furnished to this specification shall include the following items:

5.1.1 Crystal Growth Method (see Section 6.1 and Note 1).

5.1.2 Conductivity Type and Dopant (see Note 1).

5.1.3 Resistivity or Resistivity Range.

5.1.4 Lot Acceptance Procedures (see Section 7).

5.1.5 Test methods for specified attributes (see Section 8).

5.1.6 Certification (if required) (see Section 9).

5.1.7 Packing and Package Labeling (see Section 10).

NOTE 1: The dopant, crystal growth method (for example, Czochralski or magnetic Czochralski), doping method and any subsequent heat treatments are difficult to ascertain in the finished wafers. Verification test procedures or certification of these characteristics (see Section 9) shall be agreed upon between the supplier and the purchaser.

5.2 *Optional Criteria* — The following items may also be specified in addition to those listed above if they are considered to be necessary for the application for which the wafers are to be employed (see Appendix 1).

5.2.1 Particulate contamination (localized light scatterer) requirements (see Section 6.3.3).

5.2.2 Surface defect requirements, including surface metal contamination (see Section 6.3.4).

5.2.3 *Flatness* — As specified in Appendix 1 of SEMI M1.

5.2.4 Optional wafer identification mark symbol or symbols, if any (see Section 6.3.2).

5.3 *Additional Criteria* — Any additional criteria considered to be necessary for the application for which the wafers are to be employed may also be specified (see Appendix 1).

5 Both Japanese editions and English translations available from Japan Standards Association, 1-24, Akasaka 4-chome, Minato-ku, Tokyo 107, Japan

6 Both Japanese editions and English translations available from Japan Electronic Industry Development Association, Kikai-Shinko-Kaikan, 3-5-8 Shiba Koen, Minato-ku, Tokyo 105, Japan

7 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

6 Requirements

6.1 *Materials and Manufacture* — The material shall consist of wafers cut from ingots grown by either the normal Czochralski or the magnetic Czochralski method, at the supplier's option.

6.2 *Dimensions and Permissible Variations* — The material shall conform to the dimensions and dimensional tolerances as specified for the attributes listed in Table 1.

Table 1 Dimensional and Orientation Requirements

<i>Property</i>	<i>Target</i>	<i>Tolerance</i>	<i>Units</i>
DIAMETER	300.00	± 0.20	mm
THICKNESS, CENTER POINT	775	± 25	μm
WARP, MAX	100		μm
NINE-POINT THICKNESS VARIATION, MAX	10		μm
NOTCH (see Figure 1)			
Depth	1.00	$+ 0.25, - 0.00$	mm
Angle	90	$+ 5, - 1$	degree
BACK SURFACE FINISH (GLOSS)	≥ 0.80 times that of mirror polished silicon wafer front surface measured with a 60° angle of incidence and visible illumination		
EDGE PROFILE COORDINATE, C_y (see Figure 2 and Section 6.2.5.1)	258		μm
EDGE PROFILE SURFACE FINISH	POLISHED		
FQA RADIUS	147		mm
SURFACE ORIENTATION	{100}	$\pm 1^\circ$	
FIDUCIAL AXIS ORIENTATION (See Section 6.2.3.1)	110	$\pm 1^\circ$	

6.2.1 *Shape* — Although the warp value specified in Table 1 is expected to be adequate for many developmental purposes, it is now recognized that warp, even with correction for gravitational sag, is not a suitable metric for specifying wafer shape for all applications.

6.2.1.1 *Sori* is an attribute that may be specified as agreed between the supplier and the purchaser in lieu of warp.

6.2.1.2 *Bow* is not specified for these wafers; whether it will be required for specification of circuit-quality 300 mm diameter wafers will depend both on the development of wafer shaping technology for these wafers and on the process needs of IC manufacturing.

6.2.2 *Flatness* — The nine-point thickness variation specified in Table 1 is not the total thickness variation (the flatness parameter GBIR, as defined in Appendix 1 of SEMI M1), because initial metrology limitations required that it be determined by a sparse (nine-point) sampling plan. If suitable metrology is available, flatness attributes, such as global flatness (e.g., GBIR or GFLR) and site flatness (e.g., SFQR, SFQD, SBIR, or SBID), may be specified as agreed upon between supplier and purchaser.

6.2.3 *Fiducial Mark* — A notch in conformance with the dimensions and tolerances of Figure 1 shall be placed on the periphery of the wafer at the end of a diameter corresponding to a $\langle 100 \rangle$ crystal direction within $\pm 1^\circ$. This diameter is called the orientation fiducial axis. For (100) wafers, the allowable equivalent $\langle 100 \rangle$ directions are $[01\bar{1}]$, $[011]$, $[0\bar{1}1]$, and $[011]$.

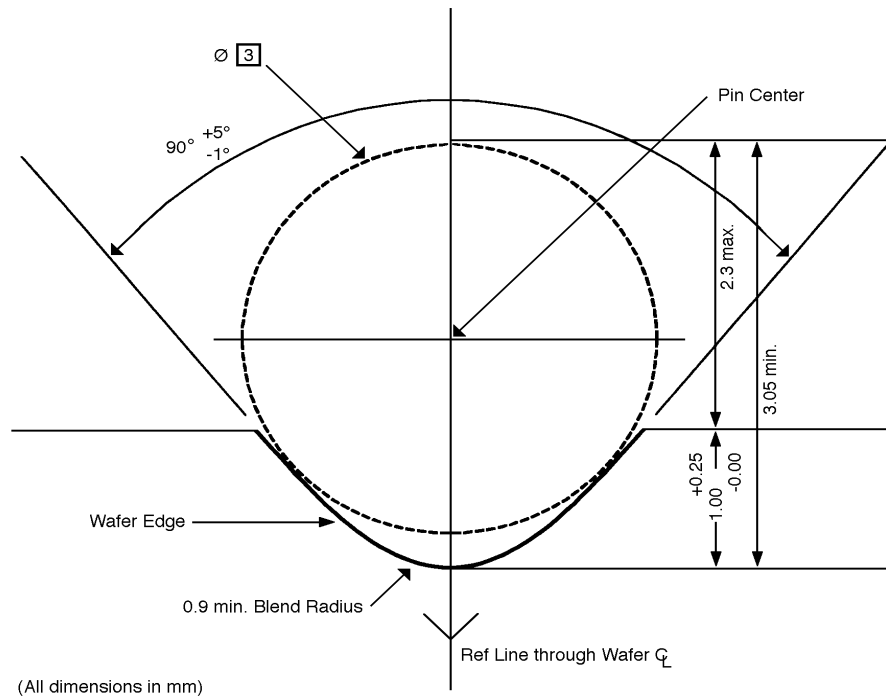


Figure 1
Notch Dimensions

6.2.3.1 No flats are permitted.

6.2.4 *Back Surface Finish* — The back surface shall have a gloss value as specified in Table 1.

6.2.5 *Edge Profile and Edge Finish* — The edge profile shall conform to the following requirements at all points on the wafer periphery (except interior portions of notches which are to be finished in accordance with the provisions of the purchase order or contract).

6.2.5.1 *Edge Profile Shape* — When the wafer is aligned with the SEMI Wafer Edge Profile Template (see Figure 2) so that the x-axis of the template is coincident with the wafer surface and the y-axis of the template is tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template. (See Figure 3 for examples of acceptable and unacceptable contours.) No sharp corners, points, or protrusions are permitted anywhere on the wafer edge contour.

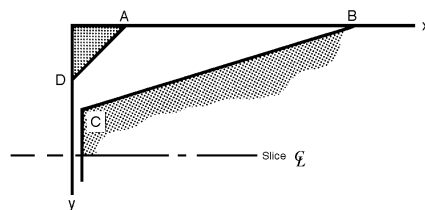


Figure 2
SEMI Wafer Edge Profile Template