

SEMI M4-1103 (Withdrawn 0307) SPECIFICATIONS FOR SOS EPITAXIAL WAFERS

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NOTICE: This document was balloted and approved for withdrawal in 2007.

1 Purpose

1.1 These specifications cover requirements for monocrystalline silicon epitaxial layers on sapphire substrates, used for semiconductor device manufacture. The combination of a silicon epitaxial layer on a sapphire substrate is known as a silicon on sapphire (SOS) epitaxial wafer. By outlining an inspection process and defining various reject criteria, both suppliers and purchasers can uniformly define epitaxial layer quality.

1.2 The defects discussed originate from two sources: those which are caused by imperfection in the sapphire substrate and those related to the epitaxial layer, including handling and packaging.

2 Scope

2.1 The primary standardized properties set forth in this specification relate to physical, dimensional, and electrical characteristics of SOS epitaxial wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards

SEMI M3 — Specifications for Polished Monocrystalline Sapphire Substrates

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF95 — Test Method for Thickness of Epitaxial Layers of Silicon on Substrates of the Same Type by Infrared Reflectance

NOTE 1: Modifications to this procedure are required for use on SOS wafers.

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-implanted Layers Using an In-Line Four-Point Probe with the Single-Configuration Procedure

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafers

SEMI MF673 — Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

3.2 ASTM Standard¹

E 122 — Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

3.3 Other Standard²

ANSI/ASQC Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

¹ American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; Website: <http://www.astm.org>

² American National Standards Institute, Headquarters: 1819 L Street, NW, Washington, DC 20036, USA. Telephone: 202.293.8020; Fax: 202.293.9287; New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023; Website: <http://www.ansi.org>

4 Terminology

4.1 Definitions

4.1.1 *deposition* — the technique involved in the vapor deposition of single-crystal silicon on oriented sapphire substrates.

4.1.2 *dopant* — a chemical element, usually from the third or fifth columns of the periodic table (typically phosphorous, arsenic, or boron), incorporated in trace amounts in the epitaxial layer to establish its conductivity type and resistivity.

4.1.3 *doping* — the process of incorporation of a dopant into the epitaxial layer while the film is growing.

4.1.4 *epitaxial layer* — the layer of semiconductor material that is grown on the substrate.

4.1.5 *lot* — for the purpose of this document, (a) all of the wafers of nominally identical specification and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of epitaxial wafers as above which have been identified by the supplier as constituting a lot.

4.1.6 *pre-epitaxial treatment* — the process of etching an amount of material from the sapphire substrate in situ prior to deposition.

NOTE 2: Hydrogen (H_2) gas is commonly used for this purpose.

4.1.7 *resistivity* ($\Omega\cdot\text{cm}$) — for the purpose of this method, the volume resistivity, the ratio of the potential gradient parallel to the current in the material to the current density.

4.1.8 *silicon source* — volatile or gaseous silicon compound.

NOTE 3: Silane (SiH_4) gas is commonly used for this purpose.

4.1.9 *substrate* — the polished sapphire slice upon which the epitaxial layer is deposited.

4.1.10 *surface defects* — refers to mechanical imperfections, SiO_2 residual dust, and other imperfections visible on the wafer surface. Some examples of surface defects are: dimples, pits, particulates, spots, scratches, smears, hillocks, and polycrystalline regions. Definitions given in SEMI MF154 shall be used.

4.1.11 *wafer, SOS epitaxial* — the combined sapphire substrate with the deposited epitaxial layer.

5 Ordering Information

5.1 Purchase orders for sapphire substrates furnished to this specification shall refer to SEMI M3.

5.2 Purchase orders for the epitaxial layer on sapphire substrates furnished to this specification shall include specifications for the following items:

5.2.1 Silicon source (if required),

5.2.2 Conductivity type and doping source,

5.2.3 Pre-epitaxial treatment (if required),

5.2.4 Thickness and thickness variation,

5.2.5 Resistivity and resistivity variation,

5.2.6 Film crystallinity,

5.2.7 Microparticulate density,

5.2.8 Surface defects and contamination,

5.2.9 Methods of test and measurements (see § 7),

5.2.10 Lot acceptance procedures (see § 8),

5.2.11 Certification (if required) (see § 9), and

5.2.12 Packing and marking (see § 10).

6 Requirements

6.1 The substrate shall conform to the requirements of SEMI M3.

6.2 The epitaxial layer shall meet the specification requirements for the following characteristics as specified in the purchase order or contract (see § 5.2).

6.2.1 Pre-epitaxial treatment (if required),

6.2.2 Thickness and thickness variation,