SEMI M41-0600
SPECIFICATION OF SILICON-ON INSULATOR (SOI) FOR POWER DEVICE/ICs

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on April 28, 2000. Initially available at www.semi.org May 2000; to be published June 2000.

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1 Purpose

1.1 This specification covers requirements for silicon-on-insulator (SOI) for semiconductor power-device/IC manufacture. By defining inspection procedures and acceptance criteria, both users and suppliers may define product characteristics and quality requirements.

2 Scope

2.1 This specification provides requirements of SOI wafers, which are used for power devices/ICs of specific voltage applications. The voltage ranges cover low voltage (40-60V), medium voltage (150-250V) and high voltage (500-600V). The specification covers physical, electrical, and surface parameters pertinent to bonded wafers.

2.2 Included in this document is a list of goals for inspection of these wafers which need to be negotiated between the users and suppliers of bonded wafers.

2.3 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M2 — Specifications for Silicon Epitaxial Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M34 — Guide for Specifying SIMOX Wafers

3.2 *ASTM Standards*[1]

F26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

F43 — Standard Test Methods for Resistivity of Semiconductor Materials

F81 — Standard Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

F84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

F110 — Standard Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

F154 — Standard Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F399 — Standard Test Method for Thickness of Heteroepitaxial or Polysilicon Layers

F523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

F533 — Standard Test Method for Thickness and Thickness Variation of Silicon Wafers

F576 — Standard Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry

F613 — Standard Test Method for Measuring Diameter of Semiconductor Wafers

F671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

F847 — Standard Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

F928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

F1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

F1153 — Standard Test Method for Characterization of Metal-Oxide-Silicon (MOS) Structures by Capacitance-Voltage Measurements

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959

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F1188 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

F1241 — Standard Terminology of Silicon Technology

F1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

F1391 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

F1526 — Standard Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence Spectroscopy

F1527 — Standard Guide for Application of Silicon Standard Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resisitivity of Silicon

F1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

F1535 — Standard Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

F1617 — Standard Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectroscopy

F1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at Brewster Angle

F1620 — Standard Practice for Calibrating a Scanning Surface Inspection System Using Monodisperse Polystyrene Latex Spheres Deposited on Polished or Epitaxial Wafer Surfaces

F1726 — Standard Guide for Analysis of Crystallographic Perfection of Silicon Wafers

F1727 — Detection of Oxidation Induced Defects in Polished Silicon Wafers

3.3 *ANSI Standard*[2]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.4 *JEIDA Standard*[3]

JEIDA-50 — Standard Specification for SOI Wafers

2 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

3 Japan Electronic Industry Development Association, Kikai-Shinko Bldg., 3-5-8 Shiba koen, Minato-ku, Tokyo 105-0011, Japan

NOTE 1: As listed or revised, all documents cited shall be the latest publications of adopted standards.

4 Terminology

4.1 Many terms relating to silicon technology are defined in ASTM Terminology F1241, "Terminology of Silicon Technology."

4.2 Other terms are defined as follows:

4.2.1 *base silicon wafer* — the silicon wafer below the insulator layer, supporting the top silicon film.

4.2.2 *bonded wafers* — defined as two silicon wafers bonded together with an insulating layer. This insulator layer is typically thermally grown silicon-dioxide.

4.2.3 *bonding interface* — the plane where the bonding between the two wafers takes place.

4.2.4 *buried oxide layer (BOX)* — the insulator layer between the two wafers when the insulator layer is silicon-dioxide.

4.2.5 *edge exclusion* — the difference in the diameter of the top silicon film and the diameter of the base silicon wafer.

4.2.6 *thickness of top silicon film* — the distance between the surface of the top silicon film and the top silicon film-buried oxide interface.

4.2.7 *top silicon film* — the silicon layer on top of the insulator film in which the semiconductor active devices are fabricated.

4.2.8 *void* — the absence of a chemical bond at the bonding interface.

5 Ordering Information

5.1 Purchase orders for bonded wafers furnished to this specification shall include the following items:

5.1.1 Substrate Characteristics for the device layer (*diameter, dopant, orientation, resistivity, Oi, etc.*)

5.1.2 Substrate Characteristics for the base wafer (*diameter, thickness, dopant, orientation, resistivity, etc.*)

5.1.3 Buried oxide thickness and thickness tolerances

5.1.4 Top silicon film thickness and thickness tolerances

5.1.5 Warp limits

5.1.6 Top silicon film OSF defect limits

5.1.7 Top silicon film carrier life time limits

5.1.8 Buried oxide defect limits

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5.1.9 Edge profile of the top silicon film and edge exclusion

5.1.10 Rotation alignment between top silicon film and the base silicon

5.1.11 Position of the bonding interface

5.1.12 Methods of test and measurements (see Sections 8 and 9)

5.1.13 Lot acceptance procedures (see Section 7)

5.1.14 Certification (if required)

5.1.15 Packing and marking (see Section 10)

NOTE 2: Verification test procedures of certification of these items shall be agreed upon between the users and the supplier (see Sections 8 and 9)

6 Requirements

6.1 The complete specifications for Overall Wafer, Top Silicon Film, Buried Oxide (BOX) and Base Silicon Wafer are listed in Tables 1 to 5.

Table 1 Silicon-on-Insulator (SOI) Specifications for Low Voltage (45-60V) Power Device (1)

Parameters (Units)	*Value*	*ASTM Test Method or Measurement Procedure*	*Acceptance*
Wafer(Overall)			
Diameter (mm)	125, 150, 200	F613-93	Note A
Thickness (µm)	(Value of regular silicon wafer) + (SOI thickness) + (Box thickness)	F533-96, F1530-94	Note A
Total Thickness Variation (µm)	Note C	F1530-94	Note C
LTV (µm)	Note C	F1530-94	Note C
Warp (µm)	≤ 100 (Note B, C, F)	F1390-92	Note C, or Certified by Wafer Manufactures
Edge Exclusion (mm)	≤ 3 (Note C)	Optical Metrology	Note C, or Certified by Wafer Manufactures
Edge Profile/Edge Profile Surface Finish	Note C	F928-93	Note C, or Certified by Wafer Manufactures
Top Silicon Film			
Thickness (µm)	2-12	Note D (F399-88)	Note C, E, Must be measured on each wafer
Surface Orientation	Note C	X-ray Diffraction (F26-87a)	Note C, or Certified by Wafer Manufactures
Resistivity (ohm-cm)	Note C	F43-93, F84-93, F1527-94	Note C, or Certified by Wafer Manufactures
Conductivity Type	Note C	F42-93	Note C, or Certified by Wafer Manufactures
Oxygen Concentration (/cm^3)	Note C	F1188-93a, F1619-95	Note C, or Certified by Wafer Manufactures
Carbon Concentration (/cm^3)	Note C	F1391-93	Note C, or Certified by Wafer Manufactures
Surface Cleanliness: Metal Contamination (/cm^2)	Note A, C	AAS, ICP-MS, TXRF (F1526-95), SIMS (F1617-98)	Note A, C
Surface Cleanliness: Particle Density (/wafer)	Note A, C	Light Scattering Tomography (F1620-96) (SEMI M34)	Note A, C
Surface Roughness (nm)	Note A, C	AFM (SEMI M34)	Note A, C

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Carrier Lifetime (µsec)	Note C	µ-PCD Method (F1535-94)	Note C
Crystalline Alignment of Top Silicon Film to Base Wafer (°)	Note C	X-ray diffraction (F847-94)	Note C
Surface Feature (Haze, Scratch, etc)	None	F154-94, F523-93, F1726-97	Must be measured on each wafer
OSF Density (/cm^2)	Note C	Optical Metrology (F1727-97)	Note C, or Certified by Wafer Manufactures
Buried Oxide (BOX)			
Thickness (µm)	0.5-2	Ellipsometry (F576-95) or Reflective Spectroscopy (SEMI M34)	Tolerance is ± 5%; Note C, or Certified by Wafer Manufactures
Location of Bonded Interface	Lower Surface (Note C)	TEM	Certified by Wafer Manufactures
Void Density (/cm^2)	None	Scanning Acoustic Tomography, Optical Defect Inspection	Note C
Oxide Defect Density (/cm^2)	Note C	I-V on Capacitor, Cu Decoration (SEMI M34)	Note C
Dielectric Breakdown Voltage (V)	Note C	I-V on Capacitor	Note C
Interface States (/cm^2)	Note C, H	C-V Technique	Note C
Fixed Charge Density (/cm^2)	Note C, H	C-V Technique (F1153-92)	Note C
Bonding Strength (kg/cm^2)	Note C	Tensile Strength	Note C, or Certified by Wafer Manufactures
Base Silicon Wafer			
Crystalline Orientation	Note C	F26-87a	Note C
Resistivity (ohm-cm)	Note C	F43-93, F84-93, F1527-94	Note C
Conductivity Type	Note C	F42-93	Note C
Fiducial Axis Orientation (Flat/Notch)	Note C	F671-90, F1152-93	Note C
To-be-bonded Surface Cleanliness: Metals (/cm^2)	Note C	AAS, ICP-MS, XRF (F1526-95), SIMS (F1617-98)	Note C
Back Surface Finish	Note C	Optical Metrology	Note C

Table 2 Silicon-on-Insulator (SOI) Specifications for Low Voltage (45-60V) Power Device (2)

Parameters (Units)	*Value*	*ASTM Test Method or Measurement Procedure*	*Acceptance*
Wafer(Overall)			
Diameter (mm)	125, 150, 200	F613-93	Note A
Thickness (µm)	Note A	F533-96, F1530-94	Note A
Total Thickness Variation (µm)	Note C	F1530-94	Note C
LTV (µm)	Note C	F1530-94	Note C

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Warp (µm)	≤ 50 (Note B, C, F)	F1390-92	Note C, or Certified by Wafer Manufactures
Edge Exclusion (mm)	≤ 3 (Note C)	Optical Metrology	Note C, or Certified by Wafer Manufactures
Edge Profile / Edge Profile Surface Finish	Note C	F928-93	Note C, or Certified by Wafer Manufactures
Top Silicon Film			
Thickness (µm)	0.1-0.5	Note D	Note C, E, Must be measured on each wafer
Surface Orientation	Note C	X-ray Diffraction (F26-87a)	Note C, or Certified by Wafer Manufactures
Resistivity (ohm-cm)	Note C	F43-93, F84-93, F1527-94	Note C, or Certified by Wafer Manufactures
Conductivity Type	Note C	F42-93	Note C, or Certified by Wafer Manufactures
Oxygen Concentration (/cm^3)	Note C	F1188-93a, F1619-95	Note C, or Certified by Wafer Manufactures
Carbon Concentration (/cm^3)	Note C	F1391-93	Note C, or Certified by Wafer Manufactures
Surface Cleanliness: Metal Contamination (/cm^2)	Note A, C	AAS, ICP-MS, TXRF (F1526-95), SIMS (F1617-98)	Note A, C
Surface Cleanliness: Particle Density (/wafer)	Note A, C	Light Scattering Tomography (F1620-96) (SEMI M34)	Note A, C
Surface Roughness (nm)	Note A, C	AFM (SEMI M34)	Note A, C
Carrier Lifetime (µsec)	Note C	µ-PCD Method (F1535-94)	Note C
Crystalline Alignment of Top Silicon Film to Base Wafer (°)	Note C	X-ray Diffraction (F847-94)	Note C
Surface Feature (Haze, Scratch, etc)	None	F154-94, F523-93, F1726-97 (SEMI M34)	Must be measured on each wafer
Buried Oxide (BOX)			
Thickness (µm)	0.4-1.0	Ellipsometry (F576-95) or Reflective Spectroscopy (SEMI M34)	Tolerance is ± 5%; Note C, or Certified by Wafer Manufactures
Location of Bonded Interface	Lower Surface (Note C)	TEM	Certified by Wafer Manufactures
Void Density (/cm^2)	None	Scanning Acoustic Tomography, Optical Defect Inspection	Note C
Oxide Defect Density (/cm^2)	Note C	I-V on Capacitor, Cu Decoration (SEMI M34)	Note C
Dielectric Breakdown Voltage (V)	Note C	I-V on Capacitor	Note C
Interface States (/cm^2)	Note C, H	C-V Technique	Note C
Fixed Charge Density (/cm^2)	Note C, H	C-V Technique (F1153-92)	Note C

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