

SEMI M41-0707

SPECIFICATION OF SILICON-ON-INSULATOR (SOI) FOR POWER DEVICE/ICs

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1 Purpose

1.1 This specification covers requirements for silicon-on-insulator (SOI) for semiconductor power-device/IC manufacture. By defining inspection procedures and acceptance criteria, both users and suppliers may define product characteristics and quality requirements.

2 Scope

2.1 This specification provides requirements of SOI wafers, which are used for power devices/ICs of specific voltage applications. The voltage ranges cover low voltage (40–60V), medium voltage (150–250V) and high voltage (500–600V). The specification covers physical, electrical, and surface parameters pertinent to bonded SOI wafers.

2.2 Included in this document is a list of goals for inspection of these wafers which need to be negotiated between the users and suppliers of bonded SOI wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M34 — Guide for Specifying SIMOX Wafers

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Polystyrene Latex Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI M59 — Terminology for Silicon Technology

SEMI M62 — Specifications for Silicon Epitaxial Wafers

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF43 — Test Methods for Resistivity of Semiconductor Materials

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF576 — Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF847 — Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1153 — Test Method for Characterization of Metal-Oxide-Silicon (MOS) Structures by Capacitance-Voltage Measurements

SEMI MF1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1527 — Guide for Application of Silicon Standard Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at Brewster Angle

SEMI MF1726 — Guide for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ASTM Standards*¹

ASTM E122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

ASTM F399 — Standard Test Method for Thickness of Heteroepitaxial or Polysilicon Layers²

3.3 *ANSI Standard*³

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.4 *ISO Standard*⁴

ISO 14706 — Surface chemical analysis — Determination of surface elemental contamination on silicon wafers by total reflection X-ray fluorescence spectroscopy (TXRF)

3.5 *JEITA Standard*⁵

JEITA EM-3603B — Standard for SOI Wafers and Metrology

¹ ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; <http://www.astm.org>

² This standard was withdrawn in 2002. Earlier editions may be available from ASTM.

³ American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

⁴ International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; <http://www.iso.ch>

⁵ Japanese Electronic and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan. Telephone: 81.3.3518.6434; Fax: 81.3.3295.8727; <http://www.jeita.or.jp>

3.6 JIS Standards⁶

H 0609 — Test methods of crystalline defects in silicon by preferential etch techniques

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 General acronyms, terms, and symbols relating to silicon technology, including those related to SOI wafers, are listed and defined in SEMI M59.

5 Ordering Information

5.1 Purchase orders for bonded SOI wafers furnished to this specification shall include the following items:

- 5.1.1 Substrate Characteristics for the device layer (diameter, dopant, orientation, resistivity, Oi, etc.),
- 5.1.2 Substrate Characteristics for the base wafer (diameter, thickness, dopant, orientation, resistivity, etc.),
- 5.1.3 Buried oxide thickness and thickness tolerances,
- 5.1.4 Top silicon film thickness and thickness tolerances,
- 5.1.5 Warp limits,
- 5.1.6 Top silicon film OSF defect limits,
- 5.1.7 Top silicon film carrier life time limits,
- 5.1.8 Buried oxide defect limits,
- 5.1.9 Edge profile of the top silicon film and non-SOI edge area,
- 5.1.10 Rotation alignment between top silicon film and the base silicon,
- 5.1.11 Position of the bonding interface,
- 5.1.12 Methods of test and measurements (see § 8 and § 9),
- 5.1.13 Lot acceptance procedures (see § 7),
- 5.1.14 Certification (if required), and
- 5.1.15 Packing and marking (see § 10).

NOTE 1: Verification test procedures of certification of these items shall be agreed upon between the users and the supplier (see § 8 and § 9).

6 Requirements

6.1 The complete specifications for Overall Wafer, Top Silicon Film, Buried Oxide (BOX) and Base silicon substrate are listed in Tables 1 to 5.

Table 1 Silicon-on-Insulator (SOI) Specifications for Low Voltage (45–60V) Power Device (1)

<i>Parameters (Units)</i>	<i>Value</i>	<i>Standard Reference or Measurement Procedure</i>	<i>Acceptance</i>
<i>Wafer (Overall)</i>			
Diameter (mm)	125, 150, 200	SEMI MF2074	#1
Thickness (μm)	(Value of regular silicon wafer) + (SOI thickness) + (Box thickness)	SEMI MF533, SEMI MF1530	#1

⁶ Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014; <http://www.jsa.or.jp>

Parameters (Units)	Value	Standard Reference or Measurement Procedure	Acceptance
Total Thickness Variation (μm)	#3	SEMI MF1530	#3
LTV (μm)	#3	SEMI MF1530	#3
Warp (μm)	≤100 (#2, #3, #6)	SEMI MF1390	#3, or Certified by Wafer Manufacturer
Non-SOI Edge Area (mm)	≤3 (#3)	Optical Metrology	#3, or Certified by Wafer Manufacturer
Edge Profile/Edge Profile Surface Finish	#3	SEMI MF928	#3, or Certified by Wafer Manufacturer
<i>Top Silicon Film</i>			
Thickness (μm)	2–12	#4 (ASTM F399)	#3, #5 Must be measured on each wafer
Surface Orientation	#3	X-ray Diffraction (SEMI MF26)	#3, or Certified by Wafer Manufacturer
Resistivity (ohm-cm)	#3	SEMI MF43, SEMI MF84, SEMI MF1527	#3, or Certified by Wafer Manufacturer
Conductivity Type	#3	SEMI MF42	#3, or Certified by Wafer Manufacturer
Oxygen Concentration (/cm ³)	#3	SEMI MF1188, SEMI MF1619	#3, or Certified by Wafer Manufacturer
Carbon Concentration (/cm ³)	#3	SEMI MF1391	#3, or Certified by Wafer Manufacturer
Surface Cleanliness: Metal Contamination (/cm ²)	#1, #3	AAS, ICP-MS, TXRF (ISO 14706), SIMS (SEMI MF1617)	#1, #3
Surface Cleanliness: Particle Density (/wafer)	#1, #3	Light Scattering Tomography (SEMI M53) (SEMI M34)	#1, #3
Surface Roughness (nm)	#1, #3	AFM (SEMI M34)	#1, #3
Carrier Lifetime (μsec)	#3	μ-PCD Method (SEMI MF1535)	#3
Crystalline Alignment of Top Silicon Film to Base Wafer (°)	#3	X-ray diffraction (SEMI MF847)	#3
Surface Feature (Haze, Scratch, etc)	#3	SEMI MF154, SEMI MF523, SEMI MF1726	Must be measured on each wafer
OSF Density (/cm ²)	#3	Optical Metrology (SEMI MF1727)	#3, or Certified by Wafer Manufacturer
<i>Buried Oxide (BOX)</i>			
Thickness (μm)	0.5–2	Ellipsometry (SEMI MF576) or Reflective Spectroscopy (SEMI M34)	Tolerance is ±5%; #3, or Certified by Wafer Manufacturer
Location of Bonded Interface	Lower Surface (#3)	TEM	Certified by Wafer Manufacturer
Void Density (/cm ²)	None	Scanning Acoustic Tomography, Optical Defect Inspection	#3

Parameters (Units)	Value	Standard Reference or Measurement Procedure	Acceptance
Oxide Defect Density (/cm ²)	#3	I-V on Capacitor, Cu Decoration (SEMI M34)	#3
Dielectric Breakdown Voltage (V)	#3	I-V on Capacitor	#3
Interface States (/cm ²)	#3, #8	C-V Technique	#3
Fixed Charge Density (/cm ²)	#3, #8	C-V Technique (SEMI MF1153)	#3
Bonding Strength (kg/cm ²)	#3	Tensile Strength	#3, or Certified by Wafer Manufacturer
Base Silicon Substrate			
Crystalline Orientation	#3	SEMI MF26	#3
Resistivity (ohm-cm)	#3	SEMI MF43, SEMI MF84, SEMI MF1527	#3
Conductivity Type	#3	SEMI MF42	#3
Fiducial Axis Orientation (Flat/Notch)	#3	SEMI MF671, SEMI MF1152	#3
To-be-bonded Surface Cleanliness: Metals (/cm ²)	#3	AAS, ICP-MS, XRF (ISO 14706), SIMS (SEMI MF1617)	#3
Back Surface Finish	#3	Optical Metrology	#3

Table 2 Silicon-on-Insulator (SOI) Specifications for Low Voltage (45–60V) Power Device (2)

Parameters (Units)	Value	Standard Reference or Measurement Procedure	Acceptance
Wafer (Overall)			
Diameter (mm)	125, 150, 200	SEMI MF2074	#1
Thickness (μm)	#1	SEMI MF533, SEMI MF1530	#1
Total Thickness Variation (μm)	#3	SEMI MF1530	#3
LTV (μm)	#3	SEMI MF1530	#3
Warp (μm)	≤50 (#2, #3, #6)	SEMI MF1390	#3, or Certified by Wafer Manufacturer
Non-SOI Edge Area (mm)	≤3 (#3)	Optical Metrology	#3, or Certified by Wafer Manufacturer
Edge Profile/Edge Profile Surface Finish	#3	SEMI MF928	#3, or Certified by Wafer Manufacturer
Top Silicon Film			
Thickness (μm)	0.1–0.5	#4	#3, #5, Must be measured on each wafer
Surface Orientation	#3	X-ray Diffraction (SEMI MF26)	#3, or Certified by Wafer Manufacturer
Resistivity (ohm-cm)	#3	SEMI MF43, SEMI MF84, SEMI MF1527	#3, or Certified by Wafer Manufacturer
Conductivity Type	#3	SEMI MF42	#3, or Certified by Wafer Manufacturer

Parameters (Units)	Value	Standard Reference or Measurement Procedure	Acceptance
Oxygen Concentration (/cm ³)	#3	SEMI MF1188, SEMI MF1619	#3, or Certified by Wafer Manufacturer
Carbon Concentration (/cm ³)	#3	SEMI MF1391	#3, or Certified by Wafer Manufacturer
Surface Cleanliness: Metal Contamination (/cm ²)	#1, #3	AAS, ICP-MS, TXRF (ISO 14706), SIMS (SEMI MF1617)	#1, #3
Surface Cleanliness: Particle Density (/wafer)	#1, #3	Light Scattering Tomography (SEMI M53) (SEMI M34)	#1, #3
Surface Roughness (nm)	#1, #3	AFM (SEMI M34)	#1, #3
Carrier Lifetime (μsec)	#3	μ-PCD Method (SEMI MF1535)	#3
Crystalline Alignment of Top Silicon Film to Base Wafer (°)	#3	X-ray Diffraction (SEMI MF847)	#3
Surface Feature (Haze, Scratch, etc)	None	SEMI MF154, SEMI MF523, SEMI MF1726 (SEMI M34)	Must be measured on each wafer
<i>Buried Oxide (BOX)</i>			
Thickness (μm)	0.4–1.0	Ellipsometry (SEMI MF576) or Reflective Spectroscopy (SEMI M34)	Tolerance is ±5%; #3, or Certified by Wafer Manufacturer
Location of Bonded Interface	Lower Surface (#3)	TEM	Certified by Wafer Manufacturer
Void Density (/cm ²)	None	Scanning Acoustic Tomography, Optical Defect Inspection	#3
Oxide Defect Density (/cm ²)	#3	I-V on Capacitor, Cu Decoration (SEMI M34)	#3
Dielectric Breakdown Voltage (V)	#3	I-V on Capacitor	#3
Interface States (/cm ²)	#3, #8	C-V Technique	#3
Fixed Charge Density (/cm ²)	#3, #8	C-V Technique (SEMI MF1153)	#3
Bonding Strength (kg/cm ²)	#3	Tensile Strength	#3, or Certified by Wafer Manufacturer
<i>Base Silicon Substrate</i>			
Crystalline Orientation	#3	SEMI MF26	#3
Resistivity (ohm-cm)	#3	SEMI MF43, SEMI MF84, SEMI MF1527	#3
Conductivity Type	#3	SEMI MF42	#3
Fiducial Axis Orientation (Flat/Notch)	#3	SEMI MF671, SEMI MF1152	#3
To-be-bonded Surface Cleanliness: Metals (/cm ²)	#3	AAS, ICP-MS, TXRF (ISO 14706), SIMS (SEMI MF1617)	#3