

SEMI M41-0723

SPECIFICATION OF SILICON-ON-INSULATOR (SOI) FOR POWER DEVICE/ICs

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and §§) the symbols are used to reference more than one section or paragraph, respectively.

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NOTICE: This Document was completely rewritten in 2022.

1 Purpose

1.1 This Specification covers requirements for silicon on insulator (SOI) for semiconductor power-device/IC manufacture. By defining inspection procedures and acceptance criteria, both users and suppliers may define product characteristics and quality requirements.

2 Scope

2.1 This Specification provides requirements of SOI wafers, which are used for power devices/ICs of specific voltage applications. The specification described here covers physical, electrical, and surface parameters of each layer along with each voltage range for wafers ≤ 200 mm and separately, the range for 300 mm wafers in Table 1 below.

Table 1 Typical Power Device Voltage Ranges and SOI Wafer Characteristics

	Wafer Size (mm)	Application	Top Si Layer Thickness ^{#1} Range (μm)	BOX Thickness Range (μm)
1	≤ 200	Low Voltage (up to 80 V) Power Device ^{#2}	0.1 to 16	0.5 to 2
2	≤ 200	Medium Voltage (up to 400 V) Power Device	2 to 10	0.5 to 3
3	≤ 200	High Voltage (up to 1200 V) Power Device	3 to 17	3 to 5
4	300	300 mm Power Device with higher digital content and memory (up to 200 V)	0.1 to 3	0.1 to 1

#1 Refers to Si thickness as delivered by wafer supplier. Thickness can be increased or decreased as part of the device build process.

#2 Optionally with buried N+ layer.

2.2 Included in this Specification is a list of goals for inspection of these wafers which need to be negotiated between users and suppliers of bonded SOI wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI 3D17 — Specification for Reference Material for Bonded Wafer Stack Void Metrology



SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of Silicon Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers with Crystal Properties

SEMI M52 — Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130 nm to 5 nm Technology Generations

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Polystyrene Latex Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI M71 — Specification for Silicon-on-Insulator (SOI) Wafers for CMOS LSI

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF43 — Test Methods for Resistivity of Semiconductor Materials

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF576 — Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1153 — Test Method for Characterization of Metal-Oxide Silicon (MOS) Structures by Capacitance-Voltage Measurements

SEMI MF1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1527 — Guide for Application of Silicon Standard Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at Brewster Angle

SEMI MF1630 — Test Method for Low Temperature FT-IR Analysis of Single Crystal Silicon for III-V Impurities

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ANSI® Standards*¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM® Standards*²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specified Precision, the Average for a Characteristic of a Lot or Process

3.4 *ISO® Standards*³

ISO 14706 — Surface Chemical Analysis — Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence (TXRF) Spectroscopy

3.5 *JEITA Standards*⁴

JEITA EM-3603B — Standard for SOI Wafers and Metrology

3.6 *JSA Standards*⁵

JIS H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Refer to the SEMI Standards Compilation of Terms (COTs) for a list of the current Abbreviations, Acronyms, Definitions, and Symbols.

5 Ordering Information

5.1 Purchase orders for bonded SOI wafers furnished to this Specification shall include the following items:

5.1.1 Substrate Characteristics for the device layer (diameter, dopant, orientation, resistivity, Oi, etc.),

5.1.2 Substrate Characteristics for the base wafer (diameter, thickness, dopant, orientation, resistivity, etc.),

5.1.3 Buried oxide (BOX) thickness and thickness variation,

5.1.4 Top silicon film thickness and thickness variation,

5.1.5 Warp limits,

5.1.6 Top silicon film oxidation-induced stacking fault (OSF) defect limits,

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, <http://www.ansi.org>. ANSI trademark is owned by American National Standards Institute.

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

³ International Organization for Standardization, ISO Central Secretariat, Chemin de Blandonnet 8, CP 401-1214 Vernier, Geneva, Switzerland; Telephone: +41.22.749.01.11, Fax: +41.22.733.34.30, <http://www.iso.org>. ISO trademark is owned by International Organization for Standardization.

⁴ Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; Telephone: +81.03.5218.1050, Fax: +81.03.5218.1070, <http://www.jeita.or.jp>.

⁵ JSA Group, Mita MT Bldg., 3-13-12 Mita, Minato-ku, Tokyo, 108-0073, Japan; Telephone: +81.50.1741.7520, Fax: +81.3.4231.8650, <http://www.jsa.or.jp>.

- 5.1.7 Top silicon film carrier lifetime limits,
- 5.1.8 BOX defect limits,
- 5.1.9 Edge profile of the top silicon film and non-SOI edge area,
- 5.1.10 Rotational alignment between top silicon film and the base silicon,
- 5.1.11 Position of the bonding interface,
- 5.1.12 Methods of test and measurements (refer to § 8),
- 5.1.13 Lot acceptance procedures (refer to § 7),
- 5.1.14 Certification (if required), and
- 5.1.15 Packing and marking (refer to § 9).

NOTE 1: Verification test procedures of certification of these items should be agreed upon between the users and the supplier (refer to § 8).

6 Requirements

6.1 The complete specifications for overall wafer, top silicon film, BOX, and base silicon substrate are listed in Tables 2 and 3.

Table 2 Silicon-on-Insulator (SOI) Specifications for Wafers up to 200 mm

	Parameter	Typical Value	Standard Reference or Measurement Procedure	Acceptance
2.1	SOI Wafer (Overall)			
2.1.1	Diameter	125, 150, 200 mm	SEMI M1, SEMI MF2074	#1
2.1.2	Thickness	(Value of standard silicon wafer) + (Top silicon layer thickness) + (BOX thickness)	SEMI MF533, SEMI MF1530, SEMI M1	#1
2.1.3	Total thickness variation (TTV)	#3	SEMI MF1530	#3
2.1.4	Warp	#2, #3	SEMI MF1390	#3
2.1.5	Site flatness	#3	SEMI MF1530	#3
2.1.6	Non-SOI edge area (mm)	≤1 to 3 mm #3	Optical metrology	#3, or certified by wafer manufacturer
2.1.7	Wafer identification (ID) mark	#1, #3	SEMI M12, SEMI M13	#3
2.1.8	Slip	None#3	Visual (SEMI MF523), Optical metrology	#3, or certified by wafer
2.1.9	Edge exclusion (nominal)	3 to 5 mm #3	¶ 8.1	#3, or certified by wafer manufacturer
2.2	Top Silicon Layer			
2.2.1	Thickness	#3	§ 8.2	#3, #5, must be measured on each wafer
2.2.1.1	For low voltage (up to 80 V)	0.1 to 16 µm		
2.2.1.2	For medium voltage (up to 400 V)	2 to 10 µm		
2.2.1.3	For high voltage (up to 1200 V)	3 to 17 µm		
2.2.2	Thickness variation within wafer	< ±5% of top Si layer thickness or ±0.3 µm, whichever is smaller #3	§ 8.3	#3, must be measured on each wafer
2.2.3	Surface orientation	(100) ±1° #3, #4	SEMI M1, X-ray diffraction (SEMI MF26)	#3, or certified by wafer manufacturer

	<i>Parameter</i>	<i>Typical Value</i>	<i>Standard Reference or Measurement Procedure</i>	<i>Acceptance</i>
2.2.4	Fiducial (flat/notch) axis orientation	<110> or <100>, tolerance $\pm 1^\circ$ #3, #4	X-ray diffraction (SEMI MF847, SEMI MF1152)	#3, or certified by wafer manufacturer
2.2.5	Resistivity	#3, #4	SEMI MF43, SEMI MF84, SEMI MF1527	#3
2.2.6	Resistivity radial gradient (RRG)	$\leq 10\%$ #1, #3, #4	SEMI MF43, SEMI MF84, SEMI MF1527	#3, or certified by wafer manufacturer
2.2.7	Conductivity type	<i>p</i> -type or <i>n</i> -type #3, #4	SEMI MF42	#3, or certified by wafer manufacturer
2.2.8	Dopant	B (<i>p</i> -type) P, As or Sb (<i>n</i> -type) #3, #4	SIMS, Low T-FTIR (SEMI MF1630)	#3, or certified by wafer manufacturer
2.2.9	Oxygen concentration	#3, #4	SEMI MF1188, SEMI MF1619	#3
2.2.10	Oxygen radial gradient	#3, #4	SEMI MF1188, SEMI MF1619	#3
2.2.11	Carbon concentration	$\leq 2.5E + 16/\text{cm}^3$ #3, #4	SEMI MF1391	#3, or certified by wafer manufacturer
2.2.12	Surface cleanliness: metal contamination	$\leq 5E + 10/\text{cm}^2$ for each atom #1, #3	AAS, ICP-MS, TXRF (ISO 14706), SIMS (SEMI MF1617)	#1, #3, or certified by wafer manufacturer
2.2.13	Voids	None >0.5 mm diameter #3	IR transmission imaging, Optical defect inspection, Acoustic microscopy	#3, or certified by wafer manufacturer
2.2.14	Bonding interface contamination	#3	¶ 8.7	SIMS
2.2.15	Bonding strength	#3	§ 8.9	Tensile strength, HF etching
2.2.16	Localized light scatterers (LLS)	#1, #3	Light scattering tomography (SEMI M53), SEMI M71	#3
2.2.17	Surface roughness	#1, #3	AFM (SEMI M71)	#3
2.2.18	Carrier lifetime	#3, #4	μ -PCD method (SEMI MF1535)	#3, measurement applied to SOI starting wafers
2.2.19	Crystalline alignment of top Silicon layer to base wafer	$\leq \pm 1^\circ$ #3	X-ray diffraction (SEMI MF847)	#3, or certified by wafer manufacturer
2.2.20	Top surface feature (haze, scratch, etc.)	None, zero #3	SEMI MF154, SEMI MF523, SEMI M71	#3, or certified by wafer manufacturer
2.2.21	HF defects	$\leq 0.5 / \text{cm}^2$ #3	Defect etching and optical microscopy (JEITA EM-3603B), SEMI MF1809	#3, or certified by wafer manufacturer
2.2.22	Secco etch defects	$\leq 500/\text{cm}^2$ #3	Defect etching and optical microscopy (JEITA EM-3603B), SEMI MF1809	#3, or certified by wafer manufacturer
2.2.23	OSF density	#3	Optical metrology (SEMI MF1727)	#3, measurement applied to SOI starting wafers