

SEMI M47-0707 (Withdrawn 1110) SPECIFICATION FOR SILICON-ON-INSULATOR (SOI) WAFERS FOR CMOS LSI APPLICATIONS

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NOTICE: This document was balloted and approved for withdrawal in 2010.

1 Purpose

1.1 This specification defines thin-layer silicon-on-insulator (SOI) wafer requirements for CMOS large scale integrated circuit (LSI) devices. In another aspect, this specification defines the generic characteristics of SIMOX and bonded SOI wafers having typically no more than 0.2 μm SOI layer thickness. By defining parameters, inspection procedures and acceptance criteria, both suppliers and customers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 This specification is specifically directed to SIMOX and bonded silicon-on-insulator wafers, which are exclusively used for LSI applications made up of CMOS devices.

2.2 A complete purchase specification requires the base silicon wafer, SOI surface and layer, and buried oxide layer properties detailed in this standard, suitable test methods for their characterization. SEMI M18 may be for purchase specification purpose.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M41 — Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Polystyrene Latex Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI M59 — Terminology for Silicon Technology

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Test Methods for Conductivity Type of Extrinsic Semiconductor Materials

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Test Methods for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at Brewster Angle

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ASTM Standard*¹

ASTM E122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

3.3 *JEITA Standards*²

JEITA EM-3602 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surface

JEITA EM-3504³ (JEIDA 61 in old version) — Standard Test Method for Interstitial Atomic Oxygen of Silicon by Infrared Absorption

JEITA EM-3505 — Height calibration in 1 nm order for AFM

3.4 *ANSI Standard*⁴

ANSI/ASQCZ1.4 — Sampling Procedure and Tables for Inspection

3.5 *ISO Standard*⁵

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy (TXRF)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 General acronyms, terms, and symbols relating to silicon technology, including those related to SOI wafers, are listed and defined in SEMI M59.

5 Ordering Information

5.1 Purchase orders for SIMOX or bonded silicon-on-insulator wafers furnished to this specification shall include the following items:

- 5.1.1 Characteristics for the SOI layer (thickness, crystal orientation, dopant, etc.),
- 5.1.2 Characteristics for the base silicon substrate (thickness, crystal orientation, dopant, etc.),
- 5.1.3 Characteristics of the buried oxide (thickness, dielectric breakdown voltage, etc.),
- 5.1.4 Misalignment of wafer orientation between the SOI layer and the handle wafer,
- 5.1.5 Sampling plan and lot acceptance procedures (see § 7),
- 5.1.6 Methods of test and measurements (see § 8).

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; <http://www.astm.org>

2 Japanese Electronic and Information Technology Industries Association, Tokyo Chamber of Commerce and Industry Bldg. 2-2, Marunouchi 3-chome, Chiyoda-ku, Tokyo 100-0005, Japan; <http://www.jeita.or.jp>

3 Since a new number is assigned, it will be published soon. Until then, an old version spec number is to be referred.

4 American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023; <http://www.ansi.org>

5 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembe, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; <http://www.iso.ch>

6 Requirement

6.1 Requirements of SOI wafers consists of a base silicon wafer specification part and an SOI wafer specification part. A base silicon wafer is specified based on a SEMI M18 format. A similar format is applied for the specification of an SOI wafer.

6.2 As a minimum, the base silicon wafer shall conform to SEMI M1 and the appropriate individual polished single crystal silicon wafer standard; (i.e., JEITA EM-3602).

6.3 SOI wafer specified items and test methods are listed in Table 1 and shall not exceed the limits as given in Table 1.

Table 1 Specification of SOI Wafers for CMOS LSI Applications

	Item	Specification Units		Standard Reference	Test Method
		SIMOX	Bonded		
Base Silicon Wafer					
1. GENERAL CHARACTERISTICS					
1.1	Growth Method	CZ	CZ		
1.2	Crystal Orientation	(100) ± 1°	(100) ± 1°	SEMI MF26	X-ray diffraction
1.3	Conductivity Type	p-type	p-type	SEMI MF42	Hot point probe
1.4	Dopant	Boron	Boron		
1.5	Edge Exclusion, Nominal	3 (mm)	3 (mm)		
2. ELECTRICAL CHARACTERISTICS					
2.1	Resistivity (Center Point)	#1	#1	SEMI MF84	4-point probe
3. CHEMICAL CHARACTERISTICS					
3.1	Oxygen Concentration	#1	#1	SEMI MF1188, SEMI MF1619, JEITA EM-3504	IR absorption
4. STRUCTURAL CHARACTERISTICS					
4.2	Slip	None	None	SEMI MF523	Visual inspection
4.3	Lineage	None	None	SEMI MF523	Visual inspection
4.4	Twin	None	None	SEMI MF523	Visual inspection
4.5	Swirl	None	None	SEMI MF523	Visual inspection
4.6	Shallow Pits	None	None	SEMI MF523	Visual inspection
5. WAFER PREPARATION CHARACTERISITICS					
5.1	Wafer ID	#1	#1		
5.4	Extrinsic Gettering Treatment	#1	#1		
6. MECHANICAL CHARACTERISTICS					
6.1	Nominal Diameter	150/200 (mm)	150/200 (mm)	SEMI MF2074	
	Diameter Tolerance	±0.2 (mm)	±0.2 (mm)	SEMI MF2074	
6.2	Primary Flat Length/ Notch Dimension	SEMI M1 or JEITA EM-3602	SEMI M1 or JEITA EM-3602		
6.3	Primary Flat/ Notch Orientation	[011] ± 1°	[011] ± 1°	SEMI MF671, SEMI MF1152	
6.6	Edge Profile	SEMI M1	SEMI M1	SEMI MF928	
6.6.1	Edge Surface Finish	#1	#1	SEMI MF928	