SEMI M49-1108
GUIDE FOR SPECIFYING GEOMETRY MEASUREMENT SYSTEMS FOR SILICON WAFERS FOR THE 130 nm TO 22 nm TECHNOLOGY GENERATIONS

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1 Purpose

1.1 This guide provides recommendations for specifying measurement systems for geometry and flatness of silicon wafers of the 130, 90, 65, 45, 32 and 22 nm technology generation as anticipated by the International Technology Roadmap for Semiconductors (ITRS) and in the forecasts of the major manufacturers of semiconductor devices. Wafer parameters as defined by SEMI M1, SEMI M8, SEMI M11, SEMI M24, or SEMI M38 are specified by customers of silicon wafer suppliers and are usually part of Certificates of Compliance. Suppliers of silicon wafers and their customers might measure these parameters using equipment provided by different manufacturers of such equipment or using different generations of equipment of one supplier. Agreement on basic features and capability of such measurement systems improves data exchange and interpretation of data as well as procurement of appropriate measurement systems.

2 Scope

2.1 This guide outlines and recommends basic specifications for systems for measuring geometry and flatness of silicon wafers of the 130, 90, 65, 45, 32 and 22 nm technology generation.

2.2 This guide applies to measurement systems used for verifying the quality parameters geometry and flatness in large scale production of bare polished or epitaxial silicon wafers the backside of which may be acid etched and/or covered by un-patterned, homogeneous layers of, for example, poly-Si or LTO (low temperature oxide). Artifacts (e.g., reference materials) for calibrating a measurement system might have different properties.

2.3 This guide also applies to measurement systems that provide only a subset of the measurement features outlined in this guide.

2.4 The guide does not apply to measurement systems used to control intermediate process steps during Si wafer manufacturing. However, it may be completely or partly used for measurement systems for those applications provided corresponding constraints are appropriately identified.

2.5 The guide also does not apply to measurement systems for SOI wafers or patterned wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards*

SEMI E5 — SEMI Equipment Communications Standard 2 Message Content (SECS-II)

SEMI E10 — Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM)

SEMI E30 — Generic Model for Communications and Control of Manufacturing Equipment (GEM)

SEMI E37 — High Speed SECS Message Services (HSMS) Generic Services

SEMI E58 — Automated Reliability, Availability, and Maintainability Standard (ARAMS): Concepts, Behavior, and Services

SEMI E89 — Guide for Measurement System Analysis (MSA)

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SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M8 — Specification for Polished Monocrystalline Test Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M38 — Specification for Polished Reclaimed Silicon Wafers

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M59 — Terminology for Silicon Technology

SEMI M62 — Specifications for Silicon Epitaxial Wafers

SEMI MF42 —Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF84 —Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF534 —Test Method for Bow of Silicon Wafers

SEMI MF657 —Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Non-contact Scanning

SEMI MF671 —Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Methods for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Non-contact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ISO Standards*[1]

ISO/IEC 8859 — Information technology – 8-bit single-byte coded graphic character sets

ISO 8879 — Information processing – Text and office systems – Standard Generalized Markup Language (SGML)

ISO 9000 — Quality management systems – Fundamentals and vocabulary

ISO 9001 — Quality management systems – Requirements

ISO/IEC 10646-1 — Information technology – Universal multiple-octet character set (UCS) – Part 1: Architecture and basic multilingual plane

ISO/IEC 10918 — Information technology – Digital compression and coding of continuous-tone still images

ISO 14644-1 — Cleanroom and associated controlled environments – Part 1: Classification of air cleanliness

1 International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; http://www.iso.ch

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3.3 *JEITA (formerly JEIDA) Standard*[2]

JEITA EM-3401 (43) — Terminology of silicon wafer flatness

3.4 *DIN Standards*[3]

DIN 50431 — Measurement of the electrical resistivity of silicon or germanium single crystals by means of the four-point-probe direct current method with collinear probe array

DIN 50432 — Determination of the conductivity type of silicon or germanium by means of rectification test or hot-probe

DIN 50441-1 — Determination of the geometric dimensions of semiconductor slices; measurement of thickness

DIN 50441-2 — Determination of the geometric dimensions of semiconductor slices; testing of edge rounding

DIN 50441-4 — Determination of the geometric dimensions of semiconductor slices; diameter and flat depth of slices

DIN 50441-5 — Determination of the geometric dimensions of semiconductor wafers; terms of shape and flatness deviation

DIN 50445 — Contactless determination of the electrical resistivity of semiconductor wafers with the eddy current method

3.5 *IEEE Standards*[4]

IEEE 754 — IEEE Standard for Binary Floating-Point Arithmetic

IEEE 802 — IEEE Standard for Local and Metropolitan Networks: Overview and Architecture

IEEE 854 — IEEE Standard Radix-Independent Floating-Point Arithmetic

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 General terms, acronyms, abbreviations and symbols associated with silicon technology and used in this standard are listed and defined in SEMI M59.

5 Recommended Specification for Geometry Measurement Systems for Silicon Wafers

5.1 The recommended specifications are structured in three sections (Tables 1–4):

- Generic Equipment Characteristics (Table 1)
- Materials to be measured (Table 2)
- Metrology Specific Equipment Characteristics (Tables 3 and 4)

5.2 Tables 1–4 contain the specifications, referenced documents, test methods, and comments. Additional explanations and discussions are provided in this section.

5.3 *Generic Equipment Characteristics (Table 1)*

5.3.1 The section "Generic Equipment Characteristics" consists of five subsections:

- Wafer handling
- Reliability
- Procedural

2 Japanese Electronic and Information Technology Industries Association, 3rd Fl., Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan. http://www.jeita.or.jp

3 Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany; http://www.din.de

4 Institute of Electrical and Electronics Engineers, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331, USA. Telephone: 732.981.0060; Fax: 732.981.1721; http://www.ieee.org

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- Documentation
- Computer/User Interface/Connectivity

5.3.2 Subsections covering "Facilities Requirements" and "Safety/Legal/Regulatory" are not included in the present document as these issues are highly user specific and dependent on national regulations.

5.4 *Materials to be Measured (Table 2)*

5.4.1 Table 2 specifies the parameters of silicon wafers that the measurement system must be capable to handle and to measure.

5.5 *Metrology Specific Equipment Characteristics (Tables 3 and 4)*

5.5.1 This section specifies the dimensional parameters of silicon wafers to be measured and to be reported by systems for measuring the geometry and flatness of wafers as well as the required spatial resolution, precision and accuracy of the measurement system.

5.5.2 The ability of a measurement system to properly measure surface features of different spatial wavelengths is affected by the spatial bandwidth of the measurement system's response function. Spatial bandwidth can be defined in many ways and is influenced by many factors beyond the scope of this document. Some of these need to be standardized.

NOTE 1: Some of these factors may need to be standardized.

5.5.3 Spatial resolution is defined by the high spatial frequency limit of the bandwidth of the measurement system's response function.

5.5.4 Low and high cut-off frequency f_{min} and f_{max} define the bandwidth of the response function of measurement systems. The cut-off frequencies correspond to an attenuation of 0.5 for the amplitude of a sinusoidal surface feature with the exception of a low pass filter ($f_{min} = 0$) for which the attenuation remains 1 at f_{min}.

5.5.5 The rate of change of the attenuation approaching the cut-off frequencies has to be larger than the rate of a Gaussian filter with the corresponding cut-off frequency.

5.5.6 This guide recommends values of f_{max} and f_{min} that the measurement system must be capable of measuring.

5.5.7 Any variations in filtering procedures applied near the FQA boundary must be described by the supplier of the measurement system.

5.5.8 The bandwidth as specified in Tables 3 and 4 is a nominal value.

5.5.9 This guide uses a hierarchy of variability levels to describe the performance of a measurement system that is calibrated and adjusted/aligned according to the supplier's procedures. The various terms are defined in SEMI M59.

5.5.9.1 Level 1 variability: standard deviation σ_1

5.5.9.2 Level 2 variability: standard deviation σ_2

5.5.9.3 Level 3 variability: standard deviation σ_3

5.5.10 In addition two levels of systematic off-set between different measurement systems are defined:

5.5.10.1 Matching tolerance (difference of means Δ_m)

5.5.10.2 Correlation (regression curve)

5.5.11 Explicitly specified in the present document are only level 3 variability σ_3 and matching tolerance Δ_m as they correspond to the utilization of measurement systems for wafer manufacturing most closely. The supplier of a specific measurement system may optionally provide specifications for level 1 and/or level 2 variability, respectively.

NOTE 2: In the absence of certified or standard reference materials matching may be tested by using appropriate wafers complying with 130 nm, 90 nm, 65, 45, 32 or 22 nm technology node specifications, as appropriate. It is recommended to test for matching with a set of samples covering the parameter range of interest.

5.5.12 Level 3 variability σ_3 and matching tolerance Δ_m are specified with respect to anticipated specifications for wafer geometry and flatness as given in Tables 3 and 4 for a reference wafer.

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5.5.13 In the present document P/T-ratios are used for specifying level 3 variability σ_3.

5.5.13.1 A P/T ratio of 30% or less is recommended in SEMI E89 for metrology equipment. Flatness characterisitics of silicon wafers are typically described by a single sided distribution with the median approaching zero, the lower specification boundary so the P/T ratio is calculated based on a 3σ criterion, instead of 6σ. Two grades are recommended for flatness and geometry measurement systems:

- Grade A: P/T <10%, $3\sigma_3$
- Grade B: P/T <20%, $3\sigma_3$

5.5.13.2 The individual measurement features a measurement system provides may be graded differently (e.g., SFQR might meet grade A, but SBIR only grade B). This has to be indicated appropriately in the measurement systems' technical specifications.

5.5.14 Matching tolerance is specified to be less or equal to 1.5× level 3 variability ($1.5\sigma_3$). This corresponds to a greater than 99% probability that the difference of any individual measurement results obtained with two different measurement systems is smaller or equal to $5\sigma_3$.

5.5.15 The target for bias is a range of $\pm 1.5\sigma_3$ with respect to a certified value provided that appropriate reference materials are available. This corresponds to a greater than 99% probability that any individual measurement is in the range of $\pm 4\sigma_3$ around the certified value when a reference material is tested.

5.5.16 Reference material with a series of surface features with appropriate height and half width is required to verify the bandwidth of a measurement system. The height of the features corresponds to the wafer specification as outlined in Tables 3 and 4.

5.5.17 The specifications of a measurement system are verified by using wafers the parameters of which are in a range, the upper limit of which corresponds to 1.5 times anticipated wafer specification, the lower limit to 0.5 of anticipated wafer specification. These are listed in Tables 3 and 4 as Reference Wafer Specifications. All reference wafers shall meet the thickness and warp requirements listed in the table but different wafers may be used to meet the flatness and nanotopography requirements. For site related specifications not all sites must fall within the range, but the appropriate sites to be tested should be indicated. In all cases, at least three wafers in the range of values for each property shall be employed in the testing.

NOTE 3: The edge region of wafers represents the most challenging area for meeting the desired performance characteristics. This is because of the larger surface geometry variations in the region near the edge (e.g., from polishing roll-off).

5.5.18 Verification of bias, matching tolerance and the various levels of variability are performed with a measurement system that has been calibrated according to the supplier's procedures and that is under statistical process control. Procedures for determining level 1, 2, and 3 variability are given in § 6 and procedures for determining matching tolerance are given in § 7.

5.5.19 Compatibility of two measurement systems is considered to be satisfactory when the specifications of the older measurement system are met with the newer measurement system operating in the emulation mode.

NOTE 4: Compatibility can be provided by a measurement mode in which filtering, spatial resolution, etc. of another, older, measurement system is imitated.

5.5.20 The quality of a correlation between different measurement systems is not specified in this guide.

6 Limited Reproducibility Tests

NOTE 5: Limited reproducibility tests such as those described in this section do not provide any indication of the various sources of variability or of their relative importance. If this type of information is desired, it is necessary to conduct a complete designed experiment with the appropriate analysis (see SEMI E89).

6.1 *General*

6.1.1 Select a single test wafer, typical of those to be measured by the measurement system (MS) being analyzed, for the test.

6.1.2 Select a number of measurements, n (where $n \geq 30$, see Note 2), to be made on the same wafer.

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NOTE 6: The use of about 30 measurements has been found to generally provide low enough measurement uncertainty. If fewer measurements are used, the measurement uncertainty is increased, but the result is frequently satisfactory. The effect of sample size on uncertainty of the determination can be estimated by assuming that the measurement errors follow a normal distribution. Then, the uncertainty, expressed as a one-sided (upper) confidence interval, *uci,* around the estimate of repeatability is:

$$uci = \hat{\sigma}_r \sqrt{\frac{n-1}{\chi^2_{n-1,\alpha}}} \tag{1}$$

where:

$\hat{\sigma}_r$ = estimate of repeatability from n measurements,

n = number of measurements made, and

$\chi^2_{n-1,\alpha}$ = value that cuts off the upper α fraction of a chi squared distribution with $n - 1$ degrees of freedom.

For example, if $n = 15$, the upper bound confidence interval is $1.46\,\hat{\sigma}_r$. With $n = 30$, it is $1.28\,\hat{\sigma}_r$, approximately a 12.5% reduction in uncertainty of the repeatability. If the n measurements are made on different measurands (e.g., on different sites on a wafer), the uncertainty is increased by a factor of $[(n-1)/(n-g)]^{1/2}$ where g is the number of groups, assumed to be of the same size.

6.1.3 Select the appropriate setup program for the measurements. The setup should be similar to that to be used by the MS in production or development, as appropriate.

6.1.4 Determine if the MS needs to be calibrated. Calibrate, if necessary, following the manufacturer's recommended procedure. Do not recalibrate during the experiment unless required by the normal operating procedure.

6.2 *Measurements* — Perform the measurements appropriate to the level of variability to be determined.

6.2.1 *Level 1 Variability* — Load the test wafer in the MS and measure the property n times under repeatability conditions without unloading it from the instrument.

6.2.2 *Level 2 Variability*

6.2.2.1 Load the test wafer in the MS and measure the property once and then unload the wafer.

6.2.2.2 Reload the wafer into the MS and measure it once again in the shortest possible time, and then unload the wafer.

6.2.2.3 Repeat ¶ 6.2.2.2 ($n - 2$) more times in the shortest possible time interval so that a total of n measurements is made, unloading and reloading the wafer between each measurement, but otherwise under nominally identical conditions with a single calibration.

6.2.3 *Level 3 Variability*

6.2.3.1 Measure the test wafer for a total of n/D times per day under the conditions described in ¶¶ 6.2.2.1 through 6.2.2.3 on each of D days for a minimum of five days.

6.3 *Calculations*

6.3.1 Calculate the sample standard deviation of the test results:

$$s = \sqrt{\frac{1}{(n-1)}\left[\sum_{k=1}^{n}(x_k - \bar{x})^2\right]} \tag{2}$$

where:

s = sample standard deviation of the test results,

n = number of measurements made,

x_k = k^{th} test result, and

$\bar{x}$ = average value of the n test results.

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