

SEMI M51-0303

TEST METHOD FOR CHARACTERIZING SILICON WAFERS BY GATE OXIDE INTEGRITY

This test method was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on January 10, 2003. Initially available at www.semi.org January 2003; to be published March 2003. Originally published July 2002.

NOTICE: This document was rewritten in its entirety in 2002.

1 Purpose

1.1 This test method describes procedures for characterizing silicon wafers to determine Gate Oxide Integrity (GOI). This test method is effective in evaluating the density of Crystal Originated Particles (COP) in polished Czochralski (CZ) silicon wafers that influence GOI.

2 Scope

2.1 This test method provides detailed procedures for characterizing silicon wafers using GOI. This test method describes standard procedures for Metal Oxide Semiconductor (MOS) fabrication, electrical measurement, analysis, and reporting.

2.2 Thermally grown gate oxide films with gate oxide thicknesses ranging from 20–25 nm and polysilicon electrodes are used as MOS capacitors. Discussion of the gate oxide thickness is given in a later section.

2.3 Time Zero Dielectric Breakdown (TZDB) is used as the electrical characterization method of MOS capacitors.

2.4 It is well known that oxygen precipitates are also a source of gate oxide defects.¹ However, this is beyond the scope of this standard because the as-received wafers contain only a small amount of oxygen precipitate.

NOTE 1: The polysilicon film can make standard test results applicable to the testing of wafers used to fabricate integrated circuits rather than other metal electrodes because polysilicon electrodes are commonly used in actual devices.

NOTE 2: The TZDB method measures oxide breakdown electric fields using MOS capacitors. The density of COPs can be estimated from a histogram of the breakdown electric field.

NOTE 3: For a detailed discussion of sample structures for this test method, the reader is referred to EIA/JEDEC Standard 35-1. In general, the three most likely sample

structures are simple planar MOS capacitors, MOS capacitors with various isolation structures (for example, local oxidation of silicon (LOCOS), shallow trench isolation (STI)), and field effect transistors (FET). For the purpose of silicon wafer characterization, the simple planar MOS capacitor structure is preferable. This is because with the various isolation structures and FET, silicon wafers sometimes receive thermal treatments during the complicated sample fabrication process. Therefore, it is questionable to look upon a measurement of one of the latter two wafers as the starting silicon wafer characterization.

NOTE 4: This standard is based on round robin results among silicon wafer manufacturers. In general, the COPs in the polished CZ silicon substrates strongly influence the TZDB histogram of the gate oxide. This GOI test method strongly depends on wafer-surface/near-surface crystal defects, contaminations, particles and cleanliness of the MOS fabrication processes environment. Cleanliness of the processes environment should be evaluated because it strongly affects the MOS characteristics. (See Section 5.2.1 and Related Information 1).

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 SEMI Standards

SEMI C3.6 — Standard for Phosphine in Cylinders 99.98% Quality (Provisional)

SEMI C3.21 — Standard for Carbon Tetrafluoride in Cylinders (Provisional)

SEMI C3.22 — Standard for Oxygen, 99.5% Quality

SEMI C3.23 — Standard for Oxygen, 99.98% Quality

SEMI C3.28 — Standard for Nitrogen, VLSI Grade in Cylinders, 99.9996% Quality

SEMI C3.41 — Standard for Oxygen, Bulk, 99.9998% Quality (Provisional)

SEMI C3.49 — Standard for Bulk Nitrogen, 99.99999% Quality (Provisional)

SEMI C3.54 — Gas Purity Guideline for Silane

¹ K. Yamabe and K. Taniguchi, "Time-Dependent Dielectric Breakdown of Thin Thermally Grown SiO₂ Films", *J. Solid State Circuits*, SC-20, 343 (1983).

SEMI C21 — Specifications and Guidelines for Ammonium Hydroxide

SEMI C27 — Specifications and Guidelines for Hydrochloric Acid

SEMI C28 — Specifications and Guidelines for Hydrochloric Acid

SEMI C30 — Specifications and Guidelines for Hydrogen Peroxide

SEMI C35 — Specifications and Guidelines for Nitric Acid

SEMI C38 — Guideline for Phosphorus Oxychloride

SEMI C41 — Specifications and Guidelines for 2-Propanol

SEMI C44 — Specifications and Guidelines for Sulphuric Acid

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

3.2 ASTM Standards²

ASTM D5127 — Standard Guide for Ultra Pure Water Used in the Electronics and Semiconductor Industry

ASTM F1241 — Terminology of Silicon Technology

ASTM F1771 — Standard Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique

3.3 EIA/JEDEC Standards^{3, 4}

EIA/JEDEC 35 — Procedure for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-2 — Test Criteria for the Wafer-Level Testing of Thin Dielectrics

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Abbreviations & Acronyms

4.1.1 COPs — Crystal Originated Particles

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

3 Electronic Industries Alliance, EIA Engineering Department, Standards Sales Office, 2001 Eye Street, NW, Washington, D.C. 20006, USA. Website: www.eia.org

4 Joint Electron Device Engineering Council, 2500 Wilson Blvd., Arlington, VA 22201, website: www.jedec.org

4.1.2 GOI — Gate Oxide Integrity

4.1.3 LOCOS — LOCal Oxidation of Silicon

4.1.4 MOS — Metal Oxide Semiconductor

4.1.5 STI — Shallow Trench Isolation

4.1.6 TZDB — Time Zero Dielectric Breakdown

4.2 Definitions

4.2.1 Many terms relating to silicon technology are defined in ASTM Terminology F1241.

4.2.2 Definitions for some additional terms are given in SEMI M1 and ASTM F1771.

4.2.3 Other terms are defined as follows:

4.2.3.1 *crystal originated particles⁵ (COPs)* — this is one of the grown-in defects of CZ silicon wafers with an octahedral structure. It was discovered as particles appeared on the silicon surface during repetitive RCA SC-1⁶ cleaning.

NOTE 5: It has been thought that COPs are one of the main origins of GOI degradation. The gate oxide formed on the silicon surface at which the COPs appear breaks down easily at the corner of an octahedral shape like a silicon trench.^{7, 8} The oxide electric field is enhanced at that place. The breakdown electric field is weakened.

4.2.3.2 *failure modes* — The breakdown failure results are summarized in terms of the range of the oxide electric field in which the breakdown occurred. One set of categories (A, B and C for TZDB) widely used^{9, 10} is as follows:

- *A mode failure:* $0 \text{ MV/cm} \leq E_{bd} < 3 \text{ MV/cm}$
- *B mode failure:* $3 \text{ MV/cm} \leq E_{bd} < 8 \text{ MV/cm}$
- *C mode failure:* $8 \text{ MV/cm} \leq E_{bd}$

NOTE 6: Discussion on failure modes:

- *A mode failure:* Initial short

5 J. Ryuta, E. Morita, T. Tanaka and Y. Shimanuki, "Crystal – Originated Singularities on Si Wafer Surface after SC1 Cleaning", *Jpn. J. Appl. Phys.* 29(1990) L1947.

6 W. Kern and D. Puotinen, "Clean Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology", *RCA Rev.*, 31, 187(1970).

7 T. Mera, J. Jablonski, K. Nagai, and M. Watanabe, "Grown-in defects in silicon crystals responsible for gate oxide integrity deterioration", *Ohyo-Buturi*, 66(7), 728 (1997).

8 K. Yamabe and K. Imai, "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation", *IEEE Trans. Electron Devices*, ED-34, 1681 (1987).

9 K. Yamabe, K. Taniguchi, and Y. Matsushita, "Thickness Dependence of Dielectric Breakdown Failure of Thermal SiO₂ Films", *Reliability Physics – 21st Annual Proceedings*, 1983, p.184.

10 K. Yamabe, Y. Ozawa, S. Nadahara, and K. Imai, "Thermally Grown Silicon Dioxide with High Reliability", in "Semiconductor Silicon 1990", ECS Proceedings Volume 90-1, pp. 349-363.

This failure mode is caused by pinholes of the oxide films formed in the gate oxide process. COPs do not cause these oxide pinholes.

- *B mode failure*: Accidental breakdown

COPs are a main origin of this failure. This failure mode influences reliability of MOS devices and MOS integrated circuits.

- *C mode failure*: Fatigue breakdown

This failure mode is partly caused by COPs, but is almost a wearout breakdown. These categories have traditionally been used for oxide thicknesses of about 20–25 nm. For thinner films, care must be taken in their use and in proper derivation of the oxide field strength as described in Related Information 1.

4.2.3.3 time zero dielectric breakdown (TZDB) — this is one of the electrical characteristics of dielectric films. This characteristic is contrasted with time dependent dielectric breakdown.^{11, 12}

4.2.3.3.1 Discussion — An applied bias, for which the oxide leakage current goes over a predetermined value, I_{bd} , is measured as a breakdown gate voltage. The breakdown electric field is defined by the gate breakdown voltage normalized by the gate oxide thickness.

5 Summary of Method

5.1 Overview — This test method involves fabricating an array of many similar MOS capacitors on silicon wafers, measuring the TZDB voltage histogram by applying step voltage to the MOS capacitors while monitoring the oxide leakage current, and estimating the dielectric breakdown defect density caused by the silicon wafers. The defect is estimated from the B-mode failure fraction. This test is for characterizing silicon wafers and is very useful in evaluating the crystal defects (mainly COPs) of mirror-polished CZ silicon wafers.

5.2 MOS Capacitor Fabrication Process — Many MOS capacitors are formed on the test wafer. The MOS capacitor fabrication process consists of wafer cleaning, thermal oxidation, polysilicon deposition, phosphorous doping, activation heat treatment, photolithography and polysilicon etching.

5.2.1 Fabrication Environment — It is necessary to fabricate MOS capacitors in a clean room environment of 1000 class or better in total quality. That is, it needs

to be confirmed that the A-mode failure rate is 10% or less. The A-mode failure depends not only on the particle density in the work environment atmosphere but also on ultra pure water, fixtures, process apparatus, clean cloths, operation rules, etc. Heavy contamination by alkaline metals, heavy metals and so on has an important effect on the TZDB of the oxide.

5.2.2 Wafer Cleaning — To characterize the as-received silicon wafers, the wafers shall not be cleaned. If they might contaminate a furnace, the wafers shall be cleaned before oxidation. In these cases, the wafers are generally cleaned by a modified RCA method⁶. The cleaning method shall be confirmed in advance so that the previously mentioned condition for the A-mode failure is met.

5.2.3 Thermal Oxidation — The gate oxide of the MOS capacitor is thermally grown. It is desirable to fix the oxidation conditions. Because the oxidation temperature influences the rate of oxidation,¹³ which influences the oxide film thickness and thus the gate oxide quality, it is recommended that the gate oxide of 20–25 nm is grown in dry oxygen ambient at 850–950°C. The addition of HCl or water vapor to the oxidation ambient can cause underestimation of the oxide defect density. As a result, one evaluation result of a gate oxide formed under a special oxidation condition cannot be compared with another obtained under standard oxidation condition. To measure oxide film thickness, a monitor wafer is oxidized together with the sample wafers. An average value of 5 or more points on the monitor wafer is adopted as the oxide thickness.

5.2.4 Electrode Formation — A polysilicon layer with a thickness of 200–400 nm and a sheet resistance of 20–50 Ω/sq is formed by low-pressure chemical vapor deposition (LP-CVD). There are generally *in-situ* and *ex-situ* phosphorous doping methods.

5.2.5 Ex-situ Phosphorous Doping — After the undoped polysilicon film is formed by the LP-CVD method, phosphorous is diffused using POCl_3 as phosphorous source.

5.2.6 In-situ Phosphorous Doping — The phosphorous-doped polysilicon is deposited using an *in-situ* doping LP-CVD, followed by a heat treatment to activate the doped phosphorus.

NOTE 7: If the resistance of the polysilicon electrode films is too high, the voltage drop that results within the electrode cannot be neglected. In this case, the oxide leakage current is decreased in the range of the higher electric field. On the other hand, if the phosphorus doping is too high and the

11 D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", Proc. Int. Reliability Physics Symposium, 1979, p.1

12 E. S. Anolick and G. R. Nelson, "Low Field Time Dependent Dielectric Integrity", Proc. Int. Reliability Physics Symposium, 1978, p.8

13 B.E.Deal and A.S.Grove, "General relationship for the thermal Oxidation of Silicon", J.Appl.Phys., 36, 3770 (1965).

resistivity is too low, the gate oxide dielectric characteristics degrade. Too thin a polysilicon electrode makes self-healing of oxide weak spots easier. This self-healing causes the oxide breakdown defect density to be underestimated. Too thin polysilicon electrode also causes the TZDB measurement to be degraded by mechanical stress resulting from an exploring probe such as a tungsten probe. With too thick of a polysilicon electrode in the *ex-situ* doping technique, it is easy to induce a depletion layer of phosphorus near the polysilicon/SiO₂ interface that causes parasitic resistance and unnecessary voltage drop in the measurement circuit. It is desirable to monitor the thickness and sheet resistance of the polysilicon layers in every processing batch using a monitor wafer.

5.2.7 Photolithography Process — The MOS capacitors electrodes are formed by patterning in the photolithography. EIA/JEDEC Standards 35, 35-1, 35-2 are referred to regarding this mask design. The appropriate area and the appropriate number of MOS capacitors for each defect density shall be selected in order to detect crystal defects. For the evaluation of COPs, it is necessary to measure 100 or more MOS capacitors with a gate area of about 10 mm² on a wafer. (See Table R1-3 in Related Information 1.) For spares, it is desirable to prepare the plural MOS capacitors with the same gate area within each chip.

5.2.8 Etching Processes — The photo resist pattern formed by the photolithograph technique is used as a mask for polysilicon etching. Generally, either a wet etching method or a dry etching method is applied to polysilicon etching. If a wet etching method is applied, the etching rate shall be well controlled. If the peripheral oxide of the electrode is removed, it is sometimes difficult to accurately measure the TZDB. If a dry etching method is applied, especially RIE, care shall be taken with the charging-up of the MOS capacitors. In cases where the A-mode defect density is high, the MOS capacitors shall be confirmed not to be charged up during the etching process. If an ashing removal is carried out with the photo resist, care shall be taken with the charging-up of the MOS capacitors. As with RIE, in cases where the A-mode defect density is high, the MOS capacitors shall be confirmed not to be charged up during the ashing removal process. If there are oxide and polysilicon film on the backside of the wafer, those shall be removed.

5.3 Measurement of the Electrical Characteristics of MOS Capacitors

5.3.1 The dielectric breakdown defect density of silicon oxide is evaluated by the TZDB method for MOS capacitors. In the TZDB method, the gate oxide electric field of an MOS capacitor is continuously increased in stepwise fashion. The electric field applied to the gate oxide when the gate oxide leakage current exceeds the predetermined dielectric breakdown

judgment value is defined as the oxide dielectric breakdown field. From a histogram of the breakdown fields for 100 or more MOS capacitors, the dielectric breakdown defect density is estimated.

5.3.2 We can see two characteristics of the formed MOS capacitors from the current-voltage (I-V) plots. Firstly, deviation of the gate oxide thickness appears in a loose distribution of the I-V plots. Secondly, if the I-V curves bend suddenly and have gentle slope in the high voltage region, there may be high parasitic resistance, for example, high resistance in the polysilicon electrode. In such a case, the reliable measurement demands the adjustment of the MOS preparation process.

5.3.3 Applied Step Voltage

NOTE 8: For a reliable measurement, a voltage source with a well-defined output shape shall be used. An overshooting of the applied step voltage decreases the apparent oxide breakdown voltage as compared with a real breakdown voltage. In the TZDB measurement, the constant voltage is held after a predetermined period and the oxide leakage current is measured. Next, the applied voltage increases stepwise. This procedure is repeated. If the holding time is shorter than 100 ms, the voltage may not be stable enough to allow the current to be measured. 800 ms may be enough to achieve a stable voltage. Especially, in the high electric field region, the gate oxide may receive electric stress similar to time dependent dielectric breakdown (TDDB). A holding time of 200 ms is recommended. Accordingly to the round robin result as described in Related Information 1, there are no problems in setting the holding time to 100–800 ms. The recommended step height of the applied voltage is between 0.1–0.5 MV/cm in electric field. The polarity of the voltage is selected for the Si surface so as to be in accumulation. That is, for p-type silicon wafers, the gate electrodes are negatively biased. The maximum electric field is 15 MV/cm. Even if a gate voltage corresponding to more than 15 MV/cm is applied, the voltage is not effectively applied to the gate oxide because of a voltage drop due to parasitic resistance. In the case of n-type silicon wafers, the applied electrodes shall be positively biased.

5.3.4 Breakdown Judgment

5.3.4.1 The oxide dielectric breakdown is judged by the predetermined oxide leakage current. That is, when the gate oxide leakage current exceeds the dielectric breakdown judgment current, the applied voltage is defined as the breakdown voltage. The breakdown electric field is the value that the breakdown voltage is normalized by the gate oxide thickness.

5.3.4.1.1 Discussion — If the dielectric breakdown judgment current is too high ($I_g > 10^{-3}$ A), some of the proper A-mode failures can be counted as B-mode failures because of the series resistance of the samples or measurement system. Otherwise, if the dielectric breakdown judgment current is too low ($I_g < 10^{-7}$ A),

some of the proper C-mode events in which the gate oxide was not broken down are counted B-mode failures. Both cases will be taken as a mistake in the classification of the failure modes, even if the measurement is accurately done and the appropriate I-V curves measurements are achieved. A dielectric breakdown judgment current of 10^{-5} A is recommended.

6 Significance and Use

6.1 This standard gives instructions of the procedure for characterizing mirror-polished, p-type CZ silicon wafers by measuring the dielectric breakdown defect density in the thermally grown gate oxide film using the MOS capacitors. The MOS capacitors must be formed in accordance with the fabrication process described in Section 5 that influences the oxide characteristics.

6.2 It is well known that both the silicon surface morphology and the cross-sectional structure at the pattern edge of the active region of the MOS devices influences the dielectric breakdown of the gate oxide. Various kinds of contaminations also influence the dielectric breakdown of the gate oxide. Contamination

by alkaline or heavy metals and organic particles increases as the sample fabrication process progresses. Furthermore, COPs increase with increasing SC-1 treatment. These facts indicate that it is desirable to simplify the sample structure and its fabrication processes to characterize a silicon wafer by TZDB of the gate oxide. Thermal processes can cause growth of oxygen precipitates in a silicon wafer. This standard cannot be applied to silicon wafers that might receive such thermal processes.

6.3 The appropriate area and the appropriate total number of the tested MOS capacitors shall be chosen so as to answer the purpose of this standard test. For example, as shown in Table R1-3, it is suitable to select a gate electrode area of 10 mm^2 and a total number of capacitors of more than 100.

6.4 The electrode material of the MOS capacitors has a great influence on the dielectric breakdown of the gate oxide. Polysilicon is specified as the electrode material in this standard. It is applied to practical ultra large-scale integrated circuits (ULSI). The polysilicon electrode yields test results highly consistent with the actual ULSI performance.

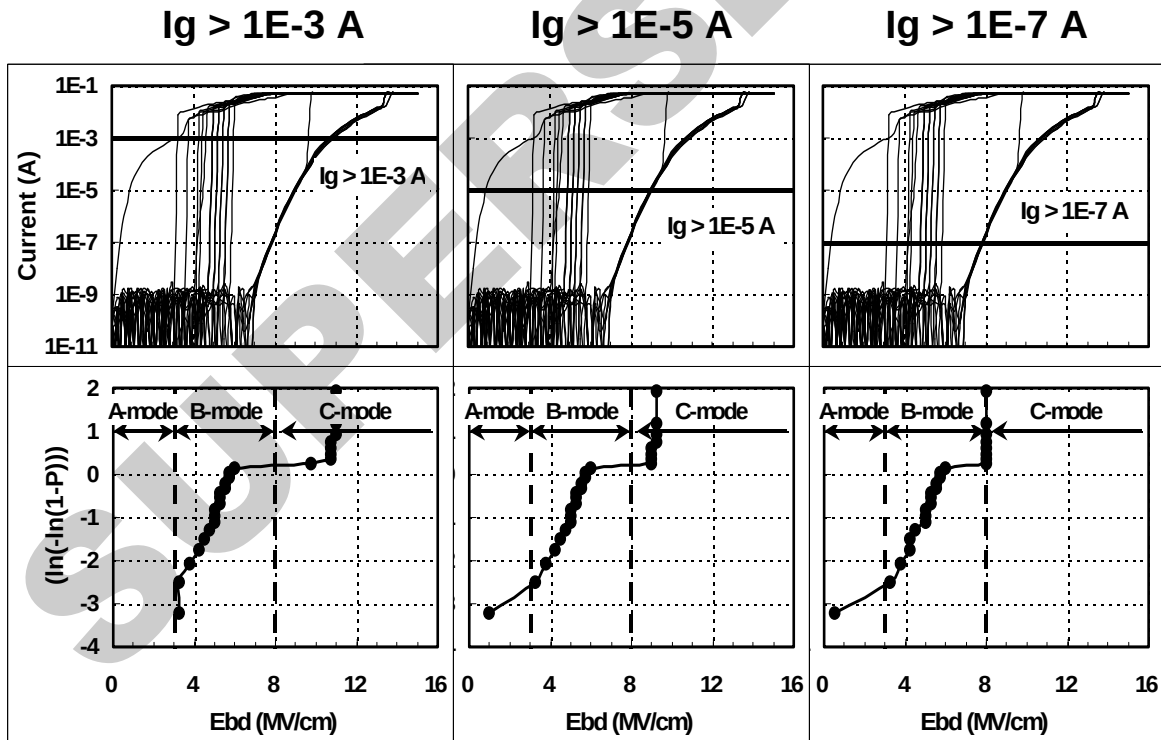


Figure 1
Comparison of Judgment Conditions