

SEMI M51-0702

TEST METHOD FOR CHARACTERIZING SILICON WAFER BY GATE OXIDE INTEGRITY

This test method was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japan Silicon Wafer Committee. Current edition approved by the Japan Regional Standards Committee on April 26, 2002. Initially available at www.semi.org June 2002; to be published July 2002.

1 Purpose

1.1 Technique outlined in this standard is for the purpose of standardizing silicon wafer characterization by Gate Oxide Integrity (GOI). For a more detailed discussion of the general characterizing methods for this test, the reader is referred to Section 3. This test method is effective to evaluating Crystal Originated Particles in polished Si wafers that influence GOI.

2 Scope

2.1 This standard is for the purpose of characterization method of silicon wafer by GOI. This characterization method outline is below.

- 1) MOS (Metal-Oxide-Semiconductor) – capacitors fabrication: On the silicon wafer surface, a gate oxide film is thermally grown. Next, poly-Si electrodes are formed on the gate oxide film.
- 2) Electrical characterization: TZDB (Time Zero Dielectric Breakdown) characteristics of the MOS capacitors are measured. The presence of COP (Crystal Originated Particles) in the polished Si substrates gives an influence of the TZDB histogram of the gate oxide. That is, the silicon wafer is characterized by such GOI methods. The technique outlined in this standard is for the purpose of standardizing the procedure of MOS fabrication, measurement, analysis, and reporting of GOI data to interested parties. This standard is based on round robin results among the silicon wafer manufacturers. In general, this GOI test strongly depends on wafer surface/near-surface crystal defects, contaminations, particles, fabrication processes, and so on. Clean environment in which the MOS capacitors are fabricated shall be evaluated to be acceptable (see Section 5.2.1 and Related Information 1).

2.2 A target of this standard is to characterize silicon wafer. A proper gate oxide thickness of the MOS sample is 20–25 nm. Discussion of the gate oxide thickness is given in later section. It is well known that oxygen precipitate is also one of the gate oxide defect

origins¹. But, this is out of discussion of this standard, because the as-received wafers contain only a little oxygen precipitate.

2.3 The poly-Si film is used as a gate electrode of measured MOS capacitors. The poly-Si film can make standard test results fitter in actual integrated circuits than other metal electrodes because the poly-Si electrode is quite commonly used in most of the actual devices. It is advisable that a poly-Si electrode thickness range is from 200 to 400 nm, and a sheet resistivity range is less than 50 ohm/sq. (These poly-Si condition is discussed in later section.)

2.4 For a detailed discussion of sample structures for this test method, the reader is referred to EIA/JEDEC Standard 35-1. In general, the three most likely sample structures are simple planner metal-oxide semiconductor (MOS) capacitors, various isolation structures (for example, local oxidation of silicon (LOCOS), shallow trench isolation (STI)), and field effect transistors (FET). For the purpose of silicon wafer characterization, the simple planner MOS capacitor structure is most desirable. In the case of the various isolation structures and FET, the silicon wafer receives thermal treatments some times in the complicated sample fabrication process. Therefore, it is questionable that we look upon this measurement as the starting Si wafer characterization.

2.5 This TZDB method measure oxide breakdown electric fields using MOS capacitors. (The measurement condition gives the details later.) The COP influence on the oxide breakdown can be estimated by histogram of breakdown electric field.

2.6 The gate voltage is negatively biased so as to be in accumulation the Si surface and be effectively applied to the gate oxide. The applied electric field is stepwise increased from 0 to 15 MV/cm (in case of 25 nm gate oxide thickness: actual applied voltage is from 0 to 37.5 V).

¹ K.Yamabe and K.Taniguchi, "Time-Dependent Dielectric Breakdown of Thin Thermally Grown SiO₂ Films", J. Solid St. Circuits, SC-20, 343(1983).

2.7 This test method is applicable to p-type CZ polished Si wafers. In the case of n-type Si wafer, the applied voltage polarity is reversed.

2.8 This standard does not purport to address safety concerns, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability or regulatory limitations prior to use.

3 Referenced Standards

NOTE 1: Unless otherwise indicated, all documents cited shall be the latest published versions.

3.1 SEMI Standards

SEMI C3.6 — Standard for Phosphine (PH₃) in Cylinders, 99.98% Quality

SEMI C3.21 — Standard for Carbon Tetrafluoride (CF₄) in Cylinders (Provisional)

SEMI C3.22 — Standard for Oxygen (O₂), 99.5% Quality

SEMI C3.23 — Standard for Oxygen (O₂), 99.98% Quality

SEMI C3.28 — Standard for Nitrogen (N₂), VLSI Grade in Cylinders, 99.9996% Quality

SEMI C3.41 — Standard for Oxygen (O₂), Bulk, 99.9998% Quality (Provisional)

SEMI C3.49 — Standard for Bulk Nitrogen (N₂), 99.99999% Quality

SEMI C3.54 — Gas Purity Guideline for Silane (SiH₄)

SEMI C21 — Specifications and Guideline for Ammonium Hydroxide

SEMI C27 — Specifications and Guidelines for Hydrochloric Acid

SEMI C28 — Specifications and Guidelines for Hydrofluoric Acid

SEMI C30 — Specifications and Guidelines for Hydrogen Peroxide

SEMI C35 — Specifications and Guideline for Nitric Acid

SEMI C38 — Guideline for Phosphorus Oxychloride

SEMI C41 — Specifications and Guidelines for 2-Propanol

SEMI C44 — Specifications and Guidelines for Sulfuric Acid

3.2 ASTM Standards²

ASTM D5127 — Standard Guide for Ultra Pure Water Used in the Electronics and Semiconductor for Industry.

ASTM F1241 — Terminology of Silicon Technology

ASTM F1771 — Standard Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique.

3.3 EIA/JEDEC Standards^{3 4}

EIA/JEDEC 35 — Procedure for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-2 — Test Criteria for the Wafer-Level Testing of Thin Dielectric

4 Terminology

4.1 Abbreviations and Acronyms

4.1.1 COP — Crystal Originated Particles

4.1.2 GOI — Gate Oxide Integrity

4.1.3 LOCOS — Local Oxidation of Silicon

4.1.4 MOS — Metal Oxide Semiconductor

4.1.5 STI — Shallow Trench Isolation

4.1.6 TZDB — Time Zero Dielectric Breakdown

4.2 Definitions

4.2.1 Many terms relating to silicon technology are defined in ASTM Terminology F 1241.

4.2.2 Definitions for some additional terms are given in SEMI M1 and ASTM F1771.

4.2.3 Other terms are defined as follows:

4.2.3.1 *crystal originated particles*⁵ (COP) — This is the one of grown-in defects in the CZ Si wafers with an octahedral structure. This was found as particles

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

3 Electronic Industries Alliance, EIA Engineering Department, Standards Sales Office, 2001 Eye Street, NW, Washington, D.C. 20006, USA. Website: www.eia.org

4 Joint Electron Device Engineering Council, 2500 Wilson Blvd., Arlington, VA 22201, website: www.jedec.org

5 J. Ryuta, E. Morita, T. Tanaka and Y. Shimanuki, "Crystal - Originated Singularities on Si Wafer Surface after SC1 Cleaning", *Jpn. J. Appl. Phys.* 29(1990) L947.

appeared on the silicon surface by repetition SC-1⁶ of RCA cleaning.

4.2.3.1.1 Discussion — It has been thought that the COP is one of the main origins of the GOI degradation. The gate oxide formed on the Si surface at which the COP appears easily breaks down at the corner of the octahedral shape like at a Si trench corner^{7,8}. This corner of octahedral structures is thinning the oxide films. The oxide electric field enhances at that place. The breakdown electric field is decreased.

4.2.3.2 failure modes — The breakdown failure results are summarized in terms of ranges of oxide electric field in which the breakdown occurred. One set of categories (A, B and C for TZDB) widely used^{9, 10} is as follows:

- *A mode failure*: $0 \text{ MV/cm} \leq E_{bd} < 3 \text{ MV/cm}$
- *B mode failure*: $3 \text{ MV/cm} \leq E_{bd} < 8 \text{ MV/cm}$
- *C mode failure*: $8 \text{ MV/cm} \leq E_{bd}$

4.2.3.2.1 Discussion

- *A mode failure*: Initial short

This failure mode is caused by pinholes of oxide films formed in the gate oxide process. The COP does not cause these oxide pinholes.

- *B mode failure*: Accidental breakdown

The COP is a main origin of this failure. This failure mode gives influence on MOS devices or MOS integrated circuits.

- *C mode failure*: Fatigue breakdown

This failure mode is partly caused by the COP, but is almost wearout breakdown. These categories have traditionally been used for oxide thickness about 20–25 nm. For thinner films, care must be taken in their use and in proper derivation of the oxide field strength as described in RELATED INFORMATION 1.

6 W. Kern and D. Puotinen, "Clean Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology", *RCA Rev.*, 31, 187(1970).

7 T. Mera, J. Jablonski, K. Nagai, and M. Watanabe, "Grown-in defects in silicon crystals responsible for gate oxide integrity deterioration", *Ohyo-Buturi*, 66(7), 728 (1997).

8 K. Yamabe and K. Imai, "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation", *IEEE Trans. Electron Devices*, ED-34, 1681 (1987).

9 K. Yamabe, K. Taniguchi, and Y. Matsushita, "Thickness Dependence of Dielectric Breakdown Failure of Thermal SiO₂ Films", *Reliability Physics – 21st Annual Proceedings*, 1983, p.184.

10 K. Yamabe, Y. Ozawa, S. Nadahara, and K. Imai, "Thermally Grown Silicon Dioxide with High Reliability", in "Semiconductor Silicon 1990", Proceedings of the 1990 Spring Meeting of The Electrochemical Society, P.349.

4.2.3.3 Time Zero Dielectric Breakdown (TZDB) — This is one of the electrical characteristics of dielectric films. This characteristic is contrasted with time dependent dielectric breakdown^{11,12}.

4.2.3.3.1 Discussion — An applied bias, for which the oxide leakage current goes over a predetermined I_{bd} , is measured as a breakdown gate voltage. The breakdown electric field is defined by the gate breakdown voltage normalized by the gate oxide thickness.

5 Summary of Method

5.1 Overview — This test method are fabricating array of the many similar MOS capacitors on silicon wafers, measuring the TZDB voltage histogram by applying step voltage to the MOS capacitors with monitoring the oxide leakage current, estimating the dielectric breakdown defect density which is caused by silicon wafers. The defect density is estimated from the B-mode failure fraction. This test method is to characterize the Si wafer and is very useful in the crystal defect (mainly COP) evaluation of mirror polished CZ Si wafer.

5.2 MOS Capacitor Fabrication Process — Many MOS capacitors are formed on the test wafer. The MOS fabrication process consists of wafer cleaning, thermal oxidation, poly-Si deposition, phosphorous doping, activation heat treatment, photolithography and etching.

5.2.1 Fabrication Environment — It is necessary to fabricate MOS capacitors in the clean room environment of 1000 or better class in total quality. That is, it needs to be confirmed that the A mode failure rate is 10% or less. The A mode failure depends not only on the particle of work environment atmosphere but also on the ultra pure water, fixtures, process apparatus, clean cloths, operation rules etc. Heavily contamination such as alkaline or heavy metal has an important effect on the TZDB of the oxide.

5.2.2 Wafer Cleaning — To characterize the as-received Si wafers, the wafers shall not be cleaned. If it might contaminate a furnace, the wafers shall be cleaned before oxidation. In these cases, the wafers are cleaned by a modified RCA method⁶, in general. The cleaning method shall be confirmed in advance that the previously mentioned condition for the A mode failure is met.

11 D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", *Proc. Int. Reliability Physics Symposium*, 1979, p.1

12 E. S. Anolick and G. R. Nelson, "Low Field Time Dependent Dielectric Integrity", *Proc. Int. Reliability Physics Symposium*, 1978, p.8

5.2.3 Thermal Oxidation — The gate oxide of the MOS capacitor is thermally grown. It is desirable to fix the oxidation conditions. Because the oxidation rate is influenced to oxidation temperature¹³ and the gate oxide quality is depend on the oxide film thickness⁹ and, strictly speaking, oxidation condition (ambient, temperature etc.). It is recommended that the gate oxide of about 20–25 nm thick is grown in dry oxygen ambient at 850–950°C. It is possible that addition of HCl or water vapor to the oxidation ambient leads to underestimate the oxide defect density. As the result, one evaluation result of the gate oxide formed in a special oxidation condition cannot be compared with that in the standard oxidation condition. To measure an oxide film thickness, a monitor wafer is oxidized with sample wafers. An average value of 5 or more points on the monitor wafer is adopted as the oxide thickness.

5.2.4 Electrode Formation — The poly-Si layer with a thickness of 200 nm–400 nm and a sheet resistance of 20–50 Ω/sq is formed by low-pressure chemical vapor deposition (LPCVD). In general, there are two type phosphorous doping methods. One is ex-situ doping, and another is in-situ doping.

5.2.4.1 Ex-situ Phosphorous Doping — After the undoped poly-Si film is deposited by the LP-CVD method, phosphorus is diffused using POCl_3 as a phosphorous source.

5.2.4.2 In-situ Phosphorous Doping — The phosphorous-doped poly-Si is deposited using an in-situ doping LPCVD, following a heat treatment to activate the doped phosphorus.

5.2.5 Discussion — Too high resistance of the poly-Si electrode films leads a voltage drop within the electrode not to be neglected. That is, in the case, the oxide leakage current is decreased in the range of the higher electric field. On the other hand, too low resistivity of them caused by higher concentration phosphorous doping leads the gate oxide dielectric characteristics to degrade. Too thin poly Si electrode leads self-healing of the oxide weak spots to be easier⁹. The self-healing makes us underestimate the oxide breakdown defect density. Too thin poly-Si electrode leads the TZDB measurement to degrade for mechanical stress of an exploring probe such as tungsten. Too thick poly-Si electrode in the ex-situ doping technique is easy to induce a depletion layer of phosphorus near the poly-Si/ SiO_2 interface that causes parasitic resistance and unnecessary voltage drop in a measurement circuit. It is desirable to monitor poly-Si thickness and sheet resistance of the poly-Si layers every processing batch using a monitor wafer.

¹³ B.E.Deal and A.S.Grove, “General relationship for the thermal Oxidation of Silicon”, J.Appl.Phys., 36, 3770(1965).

5.2.6 Photolithograph Process — The electrodes of the MOS capacitors are formed by patterning in the photolithograph. EIA/JEDEC Standard 35-1 is referred to about this mask design. The appropriate area and the appropriate number of the MOS capacitors for each defect density shall be selected to detect the crystal defect with a high sensitivity. For the evaluation of COP, it is necessary to measure 100 or more MOS capacitors with a gate area of 10 mm^2 on a wafer. (See Table R1-3 in Related Information 1.) It is desirable to prepare the plural of MOS capacitors of the same area within each chip as a spare.

5.2.7 Etching Processes — The photo resist pattern formed by photolithograph technique is used as the mask of poly-Silicon etching. Generally a wet etching method or a dry etching method is applied for poly-Silicon etching. If the wet etching method is applied, the etching rate shall be controlled well. If the peripheral oxide of the electrode is removed, it is sometimes difficult to accurately measure the TZDB. If the dry etching method is applied, especially RIE, charging-up of MOS capacitor shall be cared. In the case that the A mode defect density is high, the MOS capacitors shall be confirmed to not be charged up during the etching process. If an ashing removal of the photo resist is applied, the charging-up of MOS capacitor shall be cared. Similarly to RIE, in the case that the A mode defect density is high, the MOS capacitors shall be confirmed to not be charged up during the ashing process. If there an oxide and the poly-Si film on the wafer backside surface, those shall be removed.

5.3 Measurement of Electric Characteristic of MOS Capacitors

5.3.1 The dielectric breakdown defect density of the silicon oxide is evaluated by the TZDB method for the MOS capacitors. In the TZDB method, the gate oxide electric field of MOS capacitor is kept increasing in step. The electric field applied to the gate oxide when the gate oxide leakage current exceeds the predetermined dielectric breakdown judgment value is defined as the oxide dielectric breakdown field. From a histogram of the breakdown field for the 100 or more MOS capacitors, the dielectric breakdown defect density is estimated.

5.3.2 We can see two characteristics of the formed MOS capacitors from the current-voltage (IV) plots. First, deviation of the gate oxide thickness appears in a loose distribution of the IV plots. Second, if the I-V curves bend suddenly and have gentle slope in the high voltage region, there may be the high parasitism resistance, for example, the high resistance of the poly-Si electrode. In such a case, the low reliable

measurement demands the adjustment of the MOS preparation process.

5.3.3 Applied Step Voltage

5.3.3.1 For the reliable measurement, a voltage resource with well-defined output shape shall be used. An overshooting of the applied step voltage decreases the apparent oxide breakdown voltage as compared with a real breakdown voltage. In the TZDB measurement, the oxide leakage current is measured after holding the constant applied voltage during a predetermined time. After then, the applied voltage increases stepwise. This procedure is repeated. If the holding time is shorter than 100 ms, the stability of the voltage may be not enough for the current measurement. And if the hold time is longer than 800 ms, the stability of the voltage may be enough. Especially, in the high electric field region, the gate oxide may receive the electric stress similar to time dependent dielectric breakdown (TDDB). The holding time of 200 ms is recommended. Accordingly to the round robin result as described in RERATED INFORMATION 1, there are no problems in setting the holding time of 100–800 ms. A recommended step height of the applied voltage is between 0.1–0.5 MV/cm in electric field. The polarity of the voltage is selected for the Si surface so as to be in accumulation. That is, for P type silicon wafer, the gate oxide is

negatively applied. The maximum electric field is 15 MV/cm. Even if the gate voltage corresponding to more than 15 MV/cm is applied, the voltage is not affectively applied to the gate oxide because of the voltage drop at the parasitic resistance.

5.3.4 Breakdown Judgment

5.3.4.1 The oxide dielectric breakdown is judged by the predetermined oxide leakage current. That is, when the gate oxide leakage current exceeds the dielectric breakdown judgment current, the applied voltage is defined as the breakdown voltage. The breakdown electric field is the value that the breakdown voltage is normalized by the gate oxide thickness.

5.3.4.2 Discussion — If the dielectric breakdown judgment current is too high ($I_g > 10\text{--}3\text{A}$), one part of proper A-mode failures can be counted as the B-mode failure because of the series resistance of the samples or measurement system. Otherwise, if the judgment current is too low ($I_g < 10\text{--}7\text{A}$), one part of proper C-mode failures that the gate oxide was not broken down is counted as the B-mode failure. In both cases, it will be done to take a mistake in classification of the failure mode categories, even if the measurement is accurately done and appropriate I–V curves is gotten. So the dielectric breakdown judgment current of 10–5A is recommended.

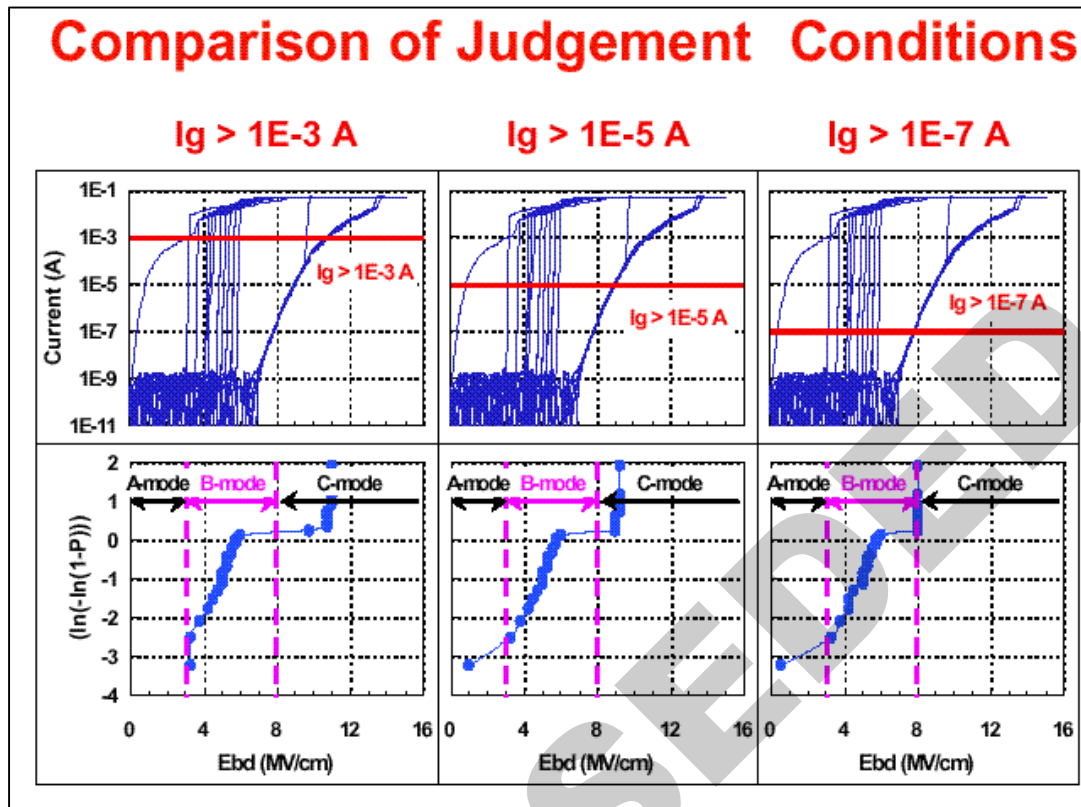


Figure 1
Comparison of Judgment Conditions

6 Significance and Use

6.1 This standard gives instructions for the procedure to characterize mirror polished CZ-grown p-type Si wafers by measuring the dielectric breakdown defect density in the thermally grown gate oxide film of the MOS capacitors. The MOS capacitors must be formed in accordance with the preparation process described in Section 5 that influences the oxide characteristics.

6.2 It is well known that both the Si surface morphology and the cross-sectional structure at the pattern edge of the active region/field isolation region of MOS devices influences the dielectric breakdown of the gate oxide. Various kinds of contaminations also influence the dielectric breakdown of the gate oxide. The contamination such as the alkaline or heavy metal and the organic particles increases with increasing sample fabrication process steps. Furthermore, the COP increases with SC-1 cleaning step numbers. These facts indicate that it is desirable to simplify the sample structure and its preparation processes to characterize the proper Si wafer by the TZDB of the gate oxide. Thermal process can cause oxygen precipitate growth in a Si wafer. This standard cannot be applied to Si wafers that might receive such a thermal process.

6.3 The appropriate area and the appropriate total number of the tested MOS capacitors shall be chosen so as to answer the purpose of this standard test. For example, as shown in Table R1-3 of RELATED INFORMATION, it is suitable to select the gate electrode area of 10 mm^2 and the total capacitor number of more than 100.

6.4 The electrode of the MOS capacitors has a great influence on the dielectric breakdown of the gate oxide. Poly-silicon is recommended as the electrode material in this standard. It is applicable to practical ultra large-scale integrated circuits (ULSI). The poly-Si electrode gives us test results highly consistent with the actual ULSI.

7 Interferences

7.1 Since this is a DC measurement, care must be taken to make sure that the Si wafer has a low resistance ohmic contact. There must be no dielectric film on the backside surface, e.g. silicon oxide, in order to effectively apply a voltage bias to the gate oxide. This is not necessary to be done with a metallic contact to the backside of the wafer under test.

7.1.1 However, when the vacuum chucking is weak, care must be taken on a possibility that the dielectric