

SEMI M51-1012

TEST METHOD FOR TIME ZERO DIELECTRIC BREAKDOWN CHARACTERISTICS OF AMORPHOUS SiO₂ FILMS FOR SILICON WAFER EVALUATION

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NOTICE: This Document was completely rewritten in 2012.

1 Purpose

1.1 This Test Method describes procedures for characterizing silicon wafers to determine gate oxide integrity (GOI). GOI is originally developed to detect crystal originated particle/pit (COP) but it is now known as a test method sensitive to other surface qualities. Therefore, the GOI evaluation results are effective information for both the wafer manufacturers and device manufacturers.

1.2 The time zero dielectric breakdown (TZDB) method can provide an oxide film failure mode classification. SEMI M60 is GOI metrology based on time dependent dielectric breakdown (TDDB) method. The TDDB method evaluates the oxide integrity.^{1,2} Therefore, the TZDB method is an important GOI metrology in addition to TDDB.

2 Scope

2.1 This Test Method provides detailed procedures for characterizing silicon wafers GOI using the TZDB method. This Test Method describes standard procedures for metal oxide semiconductor (MOS) capacitor fabrication, electrical measurement, analysis, and reporting.

2.2 Thermally grown gate oxide film with gate oxide thicknesses of 20 to 25 nm and polysilicon electrode is used to make a MOS capacitor.

2.3 It is well known that oxygen precipitates are also a source of gate oxide defects.³ However, this is beyond the scope of this Standard because the as-received wafers rarely contain oxygen precipitates large enough to impact GOI.

NOTE 1: Polysilicon electrodes can make standard test results applicable to the testing of wafers used to fabricate integrated circuits compared to other metal electrodes.

NOTE 2: TZDB method measures oxide breakdown electric fields using MOS capacitors. The density of COPs can be estimated from a histogram of the breakdown electric field.

NOTE 3: For a detailed discussion of sample structures for this Test Method, the reader is referred to JESD 35-1. In general, the three most likely MOS sample structures are simple planar MOS capacitors, MOS capacitors with various isolation structures and field effect transistors. For the purpose of silicon wafer characterization, the simple planar MOS capacitor structure is preferable.

NOTE 4: This Standard is based on round robin results among silicon wafer manufacturers. In general, the COPs in the polished CZ silicon substrates strongly influence the TZDB histogram of the gate oxide. This GOI test method strongly depends on wafer-surface/near-surface crystal defects, contaminations, particles and cleanliness of the MOS fabrication processes environment. Cleanliness of the processes environment should be carefully controlled not to deteriorate the GOI test results because it strongly affects the MOS characteristics (see ¶ 5.2.1 and Related Information 1).

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

¹ Yamabe, K., Ozawa, Y., Nadahara, S., and Imai, K. "Thermally Grown Silicon Dioxide with High Reliability." in *Semiconductor Silicon 1990*, ECS Proceedings Volume 90-1: pp. 349–63.

² Crook, D. L. "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown." *Proc. Int. Reliability Physics Symposium* (1979): p.1.

³ Yamabe, K. and Taniguchi, K. "Time-Dependent Dielectric Breakdown of Thin Thermally Grown SiO₂ Films." *J. Solid St. Circuits*, SC-20 (1983): pp. 343.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI C3.6 — Specification for Phosphine (PH₃) in Cylinders 99.98% Quality

SEMI C3.55 — Specification for Silane (SiH₄), Bulk, 99.994% Quality

SEMI C21 — Specifications and Guideline for Ammonium Hydroxide

SEMI C27 — Specifications and Guidelines for Hydrochloric Acid

SEMI C28 — Specifications for Hydrofluoric Acid

SEMI C30 — Specifications for Hydrogen Peroxide

SEMI C35 — Specifications and Guideline for Nitric Acid

SEMI C38 — Guide for Phosphorus Oxychloride

SEMI C41 — Specifications and Guidelines for 2-Propanol

SEMI C44 — Specifications and Guidelines for Sulfuric Acid

SEMI C54 — Specifications and Guidelines for Oxygen

SEMI C58 — Specifications and Guidelines for Hydrogen

SEMI C59 — Specifications and Guidelines for Nitrogen

SEMI F63 — Guide for Ultrapure Water Used in Semiconductor Processing

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI M60 — Test Method for Time Dependent Dielectric Breakdown Characteristics of SiO₂ Films for Si Wafer Evaluation

SEMI MF1771 — Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique

3.2 ASTM Standards⁴

ASTM D5127 — Standard Guide for Ultra Pure Water Used in the Electronics and Semiconductor Industries

3.3 JEDEC Standards⁵

JESD 35-A — Procedure for the Wafer-Level Testing of Thin Dielectrics

JESD 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

JESD 35-2 — Test Criteria for the Wafer-Level Testing of Thin Dielectrics

3.4 ISO Standards⁶

ISO 14644-1 — Cleanrooms and Associated Controlled Environments – Part 1: Classification of Air Cleanliness

3.5 Other Documents

JEDEC/FSA Joint Publication JP001.01⁵ — Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

⁴ ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: 610.832.9585, Fax: 610.832.9555, <http://www.astm.org>

⁵ Joint Electron Device Engineering Council, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201, USA; Telephone: 703.907.7560, Fax: 703.907.7583, <http://www.jedec.org>

⁶ International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, <http://www.iso.ch>

4 Terminology

4.1 Acronyms, terms, and symbols related to silicon technology, including those used in these practices, are listed and defined in SEMI M1 and SEMI M59.

5 Comprehensive Explanation of Terms

5.1 *COP* — It has been thought that COPs⁷ are one of the main origins of GOI degradation. The gate oxide formed on the silicon surface at which the COPs appear breaks down easily at the corner of an octahedral shape like a silicon trench as the oxide thickness becomes thinner there.^{8,9,10} The oxide electric field is enhanced at that place and the breakdown voltage becomes less.

5.2 *Failure Modes* — The breakdown failure results are summarized in terms of the range of the average oxide electric field: E_{bd} (applied voltage/oxide thickness) in which the breakdown occurred. One set of categories (A, B and C for TZDB) widely used,^{1,11} is as follows:

- *A mode failure*: $0 \text{ MV/cm} \leq E_{bd} < 3 \text{ MV/cm}$
- *B mode failure*: $3 \text{ MV/cm} \leq E_{bd} < 8 \text{ MV/cm}$
- *C mode failure*: $8 \text{ MV/cm} \leq E_{bd}$

5.2.1 Discussion on Failure Modes:

5.2.1.1 These categories have been used for oxide thicknesses between 20 to 25 nm. For thinner oxide, care must be taken in their derivation of the oxide field strength.

- *A mode failure*: Initial short — This failure mode is caused by pinholes of the oxide films formed in the gate oxide process rather than the existents of COPs.
- *B mode failure*: Accidental breakdown — COPs are a main origin of this failure. This failure mode influences reliability of MOS devices and MOS integrated circuits.
- *C mode failure*: Fatigue breakdown — This failure mode is partly caused by COPs, but mostly a wearout breakdown. For the purpose of silicon surface evaluation, this failure is not necessary to be considered.

6 Summary of Method

6.1 *Overview* — This Test Method describes fabricating an array of similar MOS capacitors on silicon wafers, and measuring the TZDB voltage. TZDB voltage is defined as the voltage when the oxide leakage current, I_g , exceeds predetermined value while applying stepwise voltage. Dielectric breakdown defect density can be derived by analyzing the histogram of TZDB distribution influenced by silicon wafer surface properties. The defect density is calculated from the B mode failure fraction. This test is useful in evaluating the silicon wafer surface quality.

6.2 *MOS Capacitor Fabrication Process* — Array of MOS capacitors are formed on the test wafer. The MOS capacitor fabrication process consists of wafer cleaning, thermal oxidation, polysilicon deposition, phosphorous doping, activation heat treatment, photolithography and polysilicon etching.

6.2.1 *Fabrication Environment* — It is necessary to fabricate MOS capacitors in a clean room environment of class 6 or better as indicated in ISO 1466-1. This means that, the A mode failure rate is 10% or less. The A mode failure depends not only on the particle density in the work environment atmosphere but also on the quality of ultra pure water, fixtures, process apparatus, clean cloths, etc. Heavy contamination by alkaline metals, heavy metals and so on has adverse effects on the TZDB.

⁷ Ryuta J., Morita E., Tanaka, T. and Shimanuki Y., “Crystal – Originated Singularities on Si Wafer Surface after SC1 Cleaning.” *Jpn. J. Appl. Phys.* 29 (1990): L1947.

⁸ Mera T., Jablonski J., Nagai K., and Watanabe M., “Grown-in defects in silicon crystals responsible for gate oxide integrity deterioration.” *Ohyo-Buturi*, 66(7), (1997): p. 728.

⁹ Yamabe K. and Imai K., “Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation.” *IEEE Trans. Electron Devices*, ED-34 (1987): p. 1681.

¹⁰ Yamabe, K., Shimada, Y., Piao, M., Yamazaki, T., Otsuki, T., Takeda, T., Ohta, Y., Jimbo, S., and Watanabe, M. “Effect of SiO₂ Thickness on Dielectric Breakdown Defect Density Due to Surface Crystal-Originated Particles.” *Journal of The Electrochemical Society*, 150, F42-F46, 2003.

¹¹ Yamabe, K., Taniguchi K., and Matsushita Y., “Thickness Dependence of Dielectric Breakdown Failure of Thermal SiO₂ Films.” *Reliability Physics – 21st Annual Proceedings* (1983): p.184.

6.2.2 Wafer Cleaning — To characterize the as-received silicon wafers, the wafers shall not be cleaned before oxidation. If the contamination of the furnace is concerned, the wafer can be cleaned. In the latter cases, the wafers are generally cleaned by a modified RCA method.¹² The adopted cleaning method shall be confirmed in advance so that the A mode failure is less than 10%.

6.2.3 Thermal Oxidation — The gate oxide of the MOS capacitor is thermally grown. It is desirable to fix the oxidation conditions. Because the oxidation temperature influences the rate of oxidation,¹³ which influences the oxide film thickness and thus the gate oxide quality, it is recommended that the gate oxide of 20 to 25 nm is grown in dry oxygen ambient at 850°C to 950°C. The addition of HCl or water vapor to the oxidation ambient can cause underestimation of the oxide defect density. As a result, one evaluation result of a gate oxide formed under a special oxidation condition cannot be compared with another obtained under standard oxidation condition. To measure oxide film thickness, a monitor wafer is oxidized together with the sample wafers. An average value of 5 or more points on the monitor wafer is adopted as the oxide thickness.

6.2.4 Gate Electrode Formation — A polysilicon layer with a thickness of 200 to 400 nm and a sheet resistance of 20 to 50 Ω is formed by low-pressure chemical vapor deposition (LP-CVD). There are generally in situ and ex situ phosphorous doping methods. It is desirable to monitor the thickness and sheet resistance of the polysilicon layers in every processing batch using a monitor wafer.

NOTE 5: Sheet Resistance Unit: The 'ohm/sq' is widely used in the semiconductor industry. This ohm/sq is not SI unit. So, in this document, it has adopted the 'ohm' which is SI unit.

6.2.4.1 Ex Situ Phosphorous Doping — After the undoped polysilicon film is formed by the LP-CVD method, phosphorous is diffused using POCl_3 as phosphorous source.

6.2.4.2 In Situ Phosphorous Doping — The phosphorous-doped polysilicon is deposited using an in situ doping LP-CVD, followed by a heat treatment to activate the doped phosphorus.

NOTE 6: If the resistance of the polysilicon electrode films is too high, the voltage drop that results within the electrode cannot be neglected. In this case, the oxide leakage current is decreased in the range of the higher electric field. On the other hand, if the phosphorus doping is too high and the resistivity is too low, the gate oxide dielectric characteristics degrade. Too thin a polysilicon electrode makes self-healing of oxide weak spots easier. This self-healing causes the oxide breakdown defect density to be underestimated. Too thin polysilicon electrode also causes the TZDB measurement to be degraded by mechanical stress resulting from an exploring probe such as a tungsten probe. With too thick of a polysilicon electrode in the ex-situ doping technique, it is easy to induce a depletion layer of phosphorus near the polysilicon/ SiO_2 interface that causes parasitic resistance and unnecessary voltage drop in the measurement circuit.

6.2.5 Photolithography Process — The MOS capacitors electrodes are formed by patterning in the photolithography. JESD 35-A, JESD 35-1, and JESD 35-2 are referred to regarding this mask design. The appropriate area and the appropriate number of MOS capacitors for each defect density shall be selected in order to detect crystal defects. For the evaluation of COPs, it is necessary to measure 100 or more MOS capacitors with a gate area of about 10 mm² on a wafer. (See Table R1-3 in Related Information 1.) For spares, it is desirable to prepare the plural MOS capacitors with the same gate area within each chip.

6.2.6 Etching Processes — The photo resist pattern formed by the photolithograph technique is used as a mask for polysilicon etching. Generally, either a wet etching method or a dry etching method is applied to polysilicon etching. If a wet etching method is applied, the etching rate shall be well controlled. If the peripheral oxide of the electrode is removed, it is sometimes difficult to accurately measure the TZDB. If a dry etching method is applied, especially RIE, care shall be taken with the charging-up of the MOS capacitors. In cases where the A-mode defect density is high, the MOS capacitors shall be confirmed not to be charged up during the etching process. If an ashing removal is carried out with the photo resist, care shall be taken with the charging-up of the MOS capacitors. As with RIE, in cases where the A-mode defect density is high, the MOS capacitors shall be confirmed not to be charged up during the ashing removal process. If there are oxide and polysilicon film on the backside of the wafer, those shall be removed.

¹² Kern, W and Puotinen, D. "Clean Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology." RCA Rev., 31, (1970): p. 187.

¹³ Deal B.E. and Grove A.S. "General relationship for the thermal Oxidation of Silicon." J.Appl.Phys., 36 (1965): p. 3770.

6.3 Measurement of the Electrical Characteristics of MOS Capacitors

6.3.1 The dielectric breakdown defect density of silicon oxide is evaluated by the TZDB method for MOS capacitors. In the TZDB method, the gate oxide electric field of an MOS capacitor is continuously increased in stepwise fashion. The electric field applied to the gate oxide when the gate oxide leakage current exceeds the predetermined dielectric breakdown judgment value is defined as the oxide dielectric breakdown field. From a histogram of the breakdown fields for 100 or more MOS capacitors, the dielectric breakdown defect density is estimated.

6.3.2 We can see two characteristics of the formed MOS capacitors from the current-voltage (I-V) plots. Firstly, deviation of the gate oxide thickness appears in a loose distribution of the I-V plots. Secondly, if the I-V curves bend suddenly and have gentle slope in the high voltage region, there may be high parasitic resistance, for example, high resistance in the polysilicon electrode. Reliable measurement requires improvement of the MOS capacitor preparation process in the case of observed high parasitic resistance.

6.3.3 Applied Step Voltage

6.3.3.1 For a reliable measurement, a voltage source with a well-defined output shape shall be used. An overshooting of the applied step voltage decreases the apparent oxide breakdown voltage as compared with a real breakdown voltage. In the TZDB measurement, the constant voltage is held after a predetermined period and the oxide leakage current is measured. Next, the applied voltage increases stepwise. This procedure is repeated. If the holding time is shorter than 100 ms, the voltage may not be stable enough to allow the current to be measured. 800 ms may be enough to achieve a stable voltage. Especially, in the high electric field region, the gate oxide may receive electric stress similar to time dependent dielectric breakdown (TDDB). A holding time of 200 ms is recommended. Accordingly to the round robin result as described in Related Information 1, there are no problems in setting the holding time to 100 to 800 ms. The recommended step height of the applied voltage is between 0.1 to 0.5 MV/cm in electric field. The polarity of the voltage is selected for the Si surface so as to be in accumulation. That is, for *p*-type silicon wafers, the gate electrodes are negatively biased. The maximum electric field is 15 MV/cm. Even if a gate voltage corresponding to more than 15 MV/cm is applied, the voltage is not effectively applied to the gate oxide because of a voltage drop due to parasitic resistance. In the case of *n*-type silicon wafers, the applied electrodes shall be positively biased.

6.3.4 Breakdown Judgment

6.3.4.1 The oxide dielectric breakdown is judged by the predetermined oxide leakage current. That is, when the gate oxide leakage current, I_g , exceeds the dielectric breakdown judgment current, the applied voltage is defined as the breakdown voltage. The breakdown electric field is the value that the breakdown voltage is normalized by the gate oxide thickness.

6.3.4.1.1 *Discussion* — If the dielectric breakdown judgment current is too high ($I_g > 10^{-3}$ A), some of the proper A-mode failures can be counted as B-mode failures because of the series resistance of the samples or measurement system. Otherwise, if the dielectric breakdown judgment current is too low ($I_g < 10^{-7}$ A), some of the proper C-mode events in which the gate oxide was not broken down are counted B-mode failures. Both cases will be taken as a mistake in the classification of the failure modes, even if the measurement is accurately done and the appropriate I-V curves measurements are achieved. A dielectric breakdown judgment current of 10^{-5} A is recommended (Figure 1).

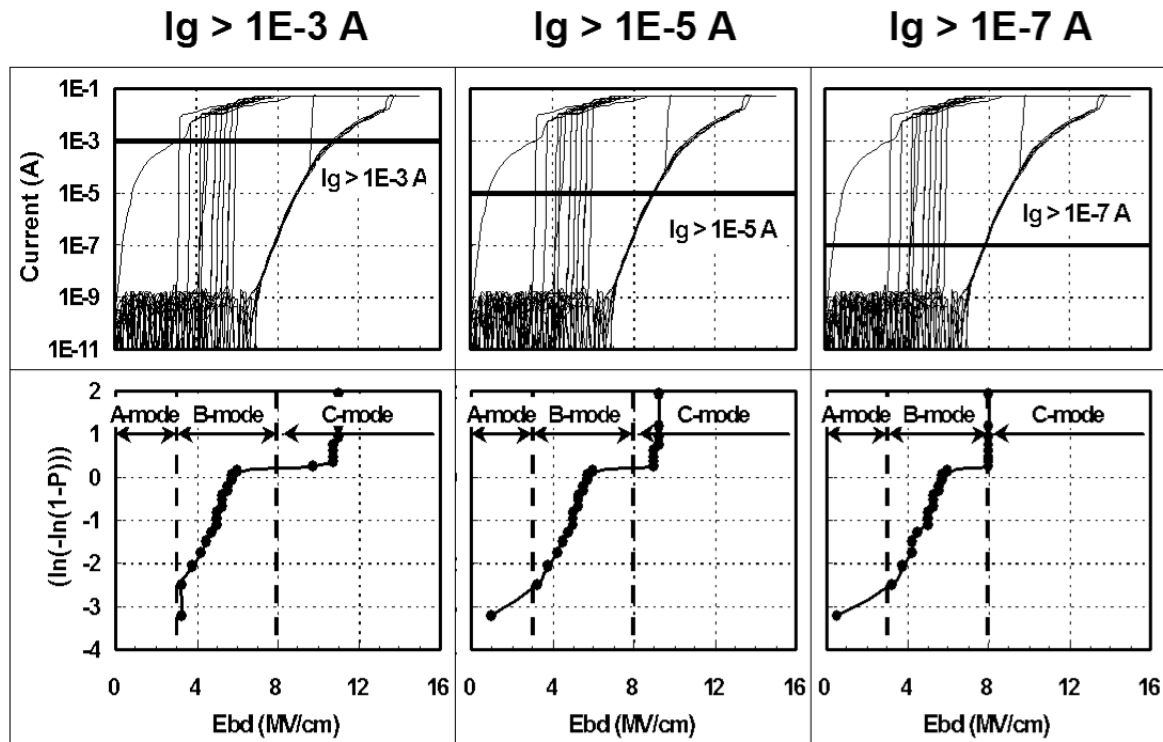


Figure 1
Comparison of Judgment Conditions

7 Significance and Use

7.1 This Standard gives instructions of the procedure for characterizing silicon wafers by measuring the dielectric breakdown defect density in the thermally grown gate oxide film using the MOS capacitors. The MOS capacitors must be formed in accordance with the fabrication process described in § 5 that influences the oxide characteristics.

7.2 It is well known that both the silicon surface morphology and the cross-sectional structure at the pattern edge of the active region of the MOS devices influence the dielectric breakdown of the gate oxide. Various kinds of contaminations also influence the dielectric breakdown of the gate oxide. Contamination by alkaline or heavy metals and organic particles increases as the sample fabrication process progresses. Furthermore, COPs increase with increasing SC-1 treatment. These facts indicate that it is desirable to simplify the sample structure and its fabrication processes to characterize a silicon wafer by TZDB of the gate oxide. Thermal processes can cause growth of oxygen precipitates in a silicon wafer. This Standard cannot be applied to silicon wafers that might receive such thermal processes.

7.3 The appropriate area and the appropriate total number of the tested MOS capacitors shall be chosen so as to answer the purpose of this standard test. For example, as shown in Table R1-3, it is suitable to select a gate electrode area of 10 mm² and a total number of capacitors of more than 100.

7.4 The electrode material of the MOS capacitors has a great influence on the dielectric breakdown of the gate oxide. Polysilicon is specified as the electrode material in this Standard.

8 Interferences

8.1 Since this is a DC measurement, care must be taken to make sure that the silicon wafer has a low resistance ohmic contact. There must be no dielectric film on the back surface; for example, silicon oxide, in order to effectively apply a voltage bias to the gate oxide. It is not necessary for this to be done with a metallic contact to the back surface of the wafer under test.