SEMI M52-0412
GUIDE FOR SPECIFYING SCANNING SURFACE INSPECTION SYSTEMS FOR SILICON WAFERS FOR THE 130 nm TO 11 nm TECHNOLOGY GENERATIONS

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1 Purpose

1.1 This Guide provides recommendations for specifying scanning surface inspection systems (SSIS) for the 130, 90, 65, 45, 32, 22, 16, and 11 nm technology generations. The number and size of localized light scatterers (LLS) on silicon wafers are specified by customers of silicon wafer suppliers and are usually part of Certificates of Compliance. Suppliers of silicon wafers and their customers might measure these parameters using measurement systems provided by different manufacturers of such systems or using different generations of measurement systems from one supplier. Therefore, standardization of various aspects of such measurement systems both improves data exchange and data interpretation and aids in procurement of appropriate measurement systems.

2 Scope

2.1 This Guide outlines and recommends basic specifications for SSIS equipment used for the 130, 90, 65, 45, 32, 22, 16, and 11 nm technology generations as driven by the 2010 edition of the International Technology Roadmap for Semiconductors (ITRS)[1] and in the forecasts of the major manufacturers of semiconductor devices.

2.2 The Guide covers generic equipment characteristics of (Table 1), materials to be measured by (Table 2), and metrology specific equipment characteristics of (Table 3) measurement systems used for verifying the quality parameter LLS counts per wafer in large scale production of bare polished or epitaxial surfaces of silicon wafers, the back surface of which may be polished or acid etched, either bare or covered by an unpatterned, homogeneous layer of polysilicon or low temperature oxide (LTO). Reference materials for calibrating measurement systems might have different properties.

2.3 The Guide also applies to measurement systems that provide only a subset of the measurement features outlined in Table 3.

2.4 This Guide does not apply to measurement systems used to control intermediate process steps during silicon wafer manufacturing. However, it may be completely or partly used for measurement systems for those applications provided corresponding constraints are appropriately identified.

2.5 This Guide does not apply to measurement systems for silicon on insulator (SOI) wafers or patterned wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI E1.9 — Mechanical Specification for Cassettes Used to Transport and Store 300 mm Wafers

SEMI E5 — SEMI Equipment Communications Standard 2 Message Content (SECS-II)

SEMI E10 — Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM)

SEMI E19 — Standard Mechanical Interface (SMIF)

[1] International SEMATECH, 2706 Montopolis Drive, Austin, TX 78741-6499, USA; Website http://www.sematech.org. Updated versions of the ITRS are available from the International SEMATECH website.

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SEMI E30 — Generic Model for Communications and Control of Manufacturing Equipment (GEM)

SEMI E37 — High Speed SECS Message Services (HSMS) Generic Services

SEMI E47 — Specification for 150 mm/200 mm Pod Handles

SEMI E47.1 — Mechanical Specification for Boxes and Pods Used to Transport and Store 300 mm Wafers

SEMI E58 — Automated Reliability, Availability, and Maintainability Standard (ARAMS): Concepts, Behavior, and Services

SEMI E89 — Guide for Measurement System Analysis (MSA)

SEMI E158 — Mechanical Specification for Fab Wafer Carrier Used to Transport and Store 450 mm Wafers (450 FOUP) and Kinematic Coupling

SEMI E159 — Mechanical Specification for Multi Application Carrier (MAC) Used to Transport and Ship 450 mm Wafers

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M31 — Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 300 mm Wafers

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M38 — Specification for Polished Reclaimed Silicon Wafers

SEMI M50 — Test Method for Determining Capture Rate and False Count Rate for Surface Scanning Inspection Systems by the Overlay Method

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI M58 — Test Method for Evaluating DMA Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

3.2 *ISO Standards*[2]

ISO 8859 — Information Technology – 8-bit Single-Byte Coded Graphic Character Sets

ISO 8879 — Information Processing – Text and Office Systems – Standard Generalized Markup Language (SGML)

ISO 9000 — Quality Management Systems – Fundamentals and Vocabulary

ISO 9001 — Quality Management Systems – Requirements

ISO 10646-1 — Information Technology – Universal Multiple-Octet Character Set (UCS) – Part 1: Architecture and Basic Multilingual Plane

ISO 10918 — Information Technology – Digital Compression and Coding of Continuous-Tone Still Images

ISO 14644-1 — Cleanroom and Associated Controlled Environments – Part 1: Classification of Air Cleanliness

ISO 14706 — Surface Chemical Analysis — Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence (TXRF) Spectroscopy (ICPMS)

[2] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, http://www.iso.ch

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3.3 *IEEE Standards*[3]

IEEE 754 — IEEE Standard for Binary Floating-Point Arithmetic

IEEE 802 — IEEE Standard for Local and Metropolitan Networks: Overview and Architecture

IEEE 854 — IEEE Standard Radix-Independent Floating-Point Arithmetic

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 General terms, acronyms, abbreviations and symbols associated with silicon technology and used in this standard are listed and defined in SEMI M59.

4.2 Other terminology required for use with this Standard is given below.

4.2.1 *classification accuracy* — the ratio of the total number of machine (SSIS) classified defects for which human and machine classification results agree to the total quantity of human classified defects.

4.2.2 *classification purity* — the ratio of the total number of machine (SSIS) classified defects for which human and machine classification results agree to the total quantity of defects classified as a specific class by the machine.

4.2.3 *slurry ring* — a ring-shaped area, higher than the surrounding wafer surface caused by incomplete cleaning of slurry residue.

4.2.4 *spike* — in an epitaxial wafer, a tall thin dendrite of crystalline filament that often occurs at the center of a recess.

5 Recommended Specifications for SSISs for Use on Silicon Wafers of the 130, 90, 65, 45, 32, 22, 16, 11 nm Technology Generations

5.1 The recommended specifications are structured in three sections (Tables 1 to 3):

- Generic Equipment Characteristics (Table 1)
- Materials to Be Measured (Table 2)
- Metrology-Specific Equipment Characteristics (Table 3)

5.1.1 Tables 1 to 3 contain the recommended specifications, referenced documents, test methods, and comments. Additional explanations and discussions are provided in this section.

5.2 *Generic Equipment Characteristics (Table 1)*

5.2.1 The section "Generic Equipment Characteristics" consists of five subsections:

- Wafer handling
- Reliability
- Procedural
- Documentation
- Computer/User Interface/Connectivity

5.2.2 Subsections covering 'Facilities Requirements' and 'Safety/Legal/Regulatory' are not included in the present guide as these issues are highly user specific and dependent on national regulations.

5.3 *Materials to Be Measured (Table 2)*

5.3.1 Table 2 and § 1 of Table 3 specify the categories and parameters of silicon wafers that the SSIS must be capable to handle and to measure.

[3] Institute of Electrical and Electronics Engineers, 3 Park Avenue, 17th Floor, New York, NY 10016-5997, USA; Telephone: 212.419.7900, Fax: 212.752.4929, http://www.ieee.org

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5.4 *Metrology Specific Equipment Characteristics (Table 3)*

5.4.1 This section specifies the measurement functions of the SSIS, the setup parameters of the SSIS, and the performance of the SSIS. Specifications in Table 3 apply to wafer front surface inspection only, except where otherwise noted.

5.4.1.1 For back surface inspection, particles, scratches, and haze are required to be detected.

5.4.2 The surface defects to be detected by the SSIS are listed in Table 3, lines 1.1.1 to 1.1.14. They are reported as LLS or extended light scatterer (XLS). The measurement performance of the system is verified with PSL sphere depositions on wafers that meet the crystal originated pit (COP) and haze requirements of the appropriate technology generation.

5.4.3 All size units of LLS are given in [length unit] LSE (e.g., nm LSE) and refer to a nominal diameter.

5.4.4 The geometrical size of a defect (LLS) may differ considerably from its size as reported in LSE units, as the cross section for light scattering of a defect depends sensitively on the properties of the LLS.

5.4.5 PSL sphere or silica spheres depositions used as reference materials are required to be certified reference materials (CRMs), traceable to a National Standards Laboratory. The characteristics of the deposition system and procedures shall be established in accordance with SEMI M58.

5.4.6 For COPs and particles, classification accuracy and purity are specified.

5.4.7 In this Guide, a hierarchy of variability levels is used to describe the performance of measurement system that is calibrated and adjusted/aligned according to the supplier's procedures. The various terms are defined in SEMI M59.

5.4.7.1 Level 1 variability: standard deviation σ_1.

5.4.7.2 Level 2 variability: standard deviation σ_2.

5.4.7.3 Level 3 variability: standard deviation σ_3.

5.4.8 In addition two levels of systematic off-set between different measurement systems are defined:

5.4.8.1 Matching tolerance (difference of means, Δ_m).

5.4.8.2 Correlation (regression curve).

5.4.9 Level 3 variability and matching tolerance are explicitly specified in Table 3.

NOTE 1: In the absence of certified or standard reference materials matching may be tested by using appropriate wafers complying with 130, 90, 65, 45, 32, 22, 16, or 11 nm technology node specifications, as appropriate. It is recommended to test for matching with a set of samples covering the parameter range of interest.

5.4.10 Procedures for determining level 1, 2, and 3 variability are given in § 6 and procedures for determining matching tolerance are given in § 7.

5.4.11 For the SSIS, downward compatibility is subject to limitations imposed by changes in geometry and number of detectors.

NOTE 2: Compatibility can be provided by a measurement mode in which filtering, spatial resolution, etc. of another, older, measurement system is imitated.

5.4.12 For sizing calibration, depositions CRMs are available from a variety of sources. On the other hand, a reference standard for the defect coordinate performance is not available.

6 Limited Reproducibility Tests

NOTE 3: Limited reproducibility tests such as those described in this section do not provide any indication of the various sources of variability or of their relative importance. If this type of information is desired, it is necessary to conduct a complete designed experiment with the appropriate analysis (see SEMI E89).

6.1 *General*

6.1.1 Select a single test wafer, typical of those to be measured by the measurement system (MS) being analyzed, for the test.

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6.1.2 Select a number of measurements, n (where n ≥ 30, see Note 4), to be made on the same wafer.

NOTE 4: The use of about 30 measurements has been found to generally provide low enough measurement uncertainty. If fewer measurements are used, the measurement uncertainty is increased, but the result is frequently satisfactory. The effect of sample size on uncertainty of the determination can be estimated by assuming that the measurement errors follow a normal distribution. Then, the uncertainty, expressed as a one-sided (upper) confidence interval, *uci,* around the estimate of repeatability is:

$$uci = \hat{\sigma}_r \sqrt{\frac{n-1}{\chi^2_{n-1,\alpha}}} \tag{1}$$

where:

$\hat{\sigma}_r$ = estimate of repeatability from *n* measurements,

n = number of measurements made, and

$\chi^2_{n-1,\alpha}$ = value that cuts off the upper α fraction of a chi squared distribution with $n - 1$ degrees of freedom.

For example, if $n = 15$, the upper bound confidence interval is $1.46\,\hat{\sigma}_r$. With $n = 30$, it is $1.28\,\hat{\sigma}_r$, approximately a 12.5% reduction in uncertainty of the repeatability. If the *n* measurements are made on different measurands (e.g., on different sites on a wafer), the uncertainty is increased by a factor of $[(n-1)/(n-g)]^{1/2}$ where *g* is the number of groups, assumed to be of the same size.

6.1.3 Select the appropriate setup program for the measurements. The setup should be similar to that to be used by the MS in production or development, as appropriate.

6.1.4 Determine if the MS needs to be calibrated. Calibrate, if necessary, following the manufacturer's recommended procedure. Do not recalibrate during the experiment unless required by the normal operating procedure.

6.2 *Measurements* — Perform the measurements appropriate to the level of variability to be determined.

6.2.1 *Level 1 Variability (Repeatability)* — Load the test wafer in the MS and measure the property *n* times under repeatability conditions without unloading it from the instrument.

6.2.2 *Level 2 Variability*

6.2.2.1 Load the test wafer in the MS and measure the property once and then unload the wafer.

6.2.2.2 Reload the wafer into the MS and measure it once again in the shortest possible time, and then unload the wafer.

6.2.2.3 Repeat ¶ 6.2.2.2 $(n - 2)$ more times in the shortest possible time interval so that a total of *n* measurements is made, unloading and reloading the wafer between each measurement, but otherwise under nominally identical conditions with a single calibration.

6.2.3 *Level 3 Variability*

6.2.3.1 Measure the test wafer for a total of *n/D* times per day under the conditions described in ¶¶ 6.2.2.1 to 6.2.2.3 on each of *D* days for a minimum of five days.

6.3 *Calculations*

6.3.1 Calculate the sample standard deviation of the test results:

$$s = \sqrt{\frac{1}{(n-1)}\left[\sum_{k=1}^{n}(x_k - \bar{x})^2\right]} \tag{2}$$

where:

s = sample standard deviation of the test results,

n = number of measurements made,

$x_k = k^{\text{th}}$ test result, and

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