SEMI M52-0703
GUIDE FOR SPECIFYING SCANNING SURFACE INSPECTION SYSTEMS FOR SILICON WAFERS FOR THE 130-nm TECHNOLOGY GENERATION

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the European Silcon Wafer Committee. Current edition approved by the European Regional Standards Committee on April 3, 2003. Initially available at www.semi.org June 2003; to be published July 2003. Originally published November 2002; previously published March 2003.

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1 Purpose

1.1 This guide provides recommendations for specifying Scanning Surface Inspection Systems (SSIS) for the 130-nm technology generation. The number and size of localized light scatterers (LLS) on silicon wafers are specified by customers of silicon wafer suppliers and are usually part of Certificates of Compliance. Suppliers of silicon wafers and their customers might measure these parameters using equipment provided by different manufacturers of such equipment or using different generations of equipment from one supplier. Therefore, standardization of various aspects of such measurement equipment both improves data exchange and data interpretation and aids in procurement of appropriate tools.

2 Scope

2.1 This guide outlines and recommends basic specifications for SSIS equipment used for the 130-nm technology generation as driven by the International Technology Roadmap for Semiconductors: 1999 edition (ITRS)[1,2] and in the forecasts of the major manufacturers of semiconductor devices.

NOTE 1: Future revisions of this Guide are expected to reflect changed requirements for the 130-nm node as well as requirements of other nodes.

2.2 The guide applies to measurement equipment used for verifying the quality parameter LLS counts per wafer in large scale production of bare polished or epitaxial surfaces of silicon wafers, the back surface of which may be polished or acid etched either bare or covered by an unpatterned, homogeneous layer of polysilicon or LTO (low temperature oxide). Artifacts (e.g reference materials) for calibrating measurement equipment might have different properties.

2.3 The guide also applies to measurement equipment that provides only a subset of the measurement features outlined in Table 3.

1 SEMATECH, 2706 Montopolis Drive, Austin, TX 78741-6499, USA Website : www.sematech.org

2 More recent versions of the ITRS are available from the homepage of International SEMATECH: www.sematech.org

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This guide does not apply to measurement equipment used to control intermediate process steps during silicon wafer manufacturing. However, it may be completely or partly used for measurement equipment for those applications provided corresponding constraints are appropriately identified.

3.2 This guide does not apply to measurement equipment for SOI wafers (Silicon on Insulators) or patterned wafers.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E1.9 — Mechanical Specification for Cassettes Used to Transport and Store 300 mm Wafers

SEMI E5 — SEMI Equipment Commuications Standard 2 Message Content (SECS-II)

SEMI E10 — Specifcation for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM)

SEMI E19 — Standard Mechanical Interface (SMIF)

SEMI E30 — Generic Model for Communications and Control of Manufacturing Equipment (GEM)

SEMI E37 — High Speed SECS Message Services (HSMS) Generic Services

SEMI E47 — Specification for 150 mm/200 mm Pod Handles

SEMI E47.1 — Provisional Mechanical Specification for Boxes and Pods Used to Transport and Store 300 mm Wafers

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SEMI E58 — Automated Reliability, Availability, and Maintainability Standard (ARAMS): Concepts, Behavior, and Services

SEMI E89 — Guide for Measurement System Capability Analysis

SEMI M1 — Specification for Polished Monocrystalline Silicon Wafers

SEMI M1.15 – Standard for 300 mm Polished Monocrystalline Silicon Wafers (Notched)

SEMI M8 — Specification for Polished Monocrystalline Silicon Test Wafers

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M31 — Provisional Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 300 mm Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M50 — Test Method for Determining Capture Rate and False Count Rate for Surface Scanning Inspection Systems by the Overlay Method

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

4.2 *ASTM Standards*[3]

ASTM F 42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

ASTM F 84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

ASTM F 154 — Practices and Nomenclature for Structures and Contaminants Seen on Specular Silicon Surfaces

ASTM F 671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

ASTM F 673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy Current Gage

ASTM F 928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

ASTM F 1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

ASTM F 1241 — Standard Terminology of Silicon Technology

ASTM F 1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Non-contact Scanning

ASTM F 1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Non-contact Scanning

ASTM F 2074 — Standard Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

4.3 *ISO Standards*[4]

ISO 8859 — Information technology – 8-bit single-byte coded graphic character sets

ISO 8879 — Information Processing – Text and office systems – Standard Generalized Markup Language (SGML)

ISO Guide 30: 1992 — Terms and definitions used in connection with reference materials

ISO 9000 — Quality management systems – Fundamentals and vocabulary

ISO 9001 — Quality management systems – Requirements

ISO 10646-1 — Information technology – Universal multiple-octet character set (UCS) – Part 1: Architecture and basic multilingual plane

ISO 10918 — Information technology – Digital compression and coding of continuous-tone still images

3 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

4 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch

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ISO 14644-1 — Cleanroom and associated controlled environments – Part 1: Classification of air cleanliness

4.4 *DIN Standards*[5]

DIN 50431 — Measurement of the electrical resistivity of silicon or germanium single crystals by means of the four-point-probe direct current method with collinear probe array

DIN 50432 — Determination of the conductivity type of silicon or germanium by means of rectification test or hot-probe

DIN 50441-1 — Determination of the geometric dimensions of semiconductor slices; measurement of thickness

DIN 50441-2 — Determination of the geometric dimensions of semiconductor slices; testing of edge rounding

DIN 50441-4 — Determination of the geometric dimensions of semiconductor slices; diameter and flat depth of slices

DIN 50441-5 — Determination of the geometric dimensions of semiconductor wafers; terms of shape and flatness deviation

DIN 50445 — Contactless determination of the electrical resistivity of semiconductor wafers with the eddy current method

4.5 *Other Standards*

IEEE 754 — IEEE Standard for Binary Floating-Point Arithmetic[6]

IEEE 802 — IEEE Standard for Local and Metropolitan Networks: Overview and Architecture[6]

IEEE 854 — IEEE Standard Radix-Independent Floating-Point Arithmetic[6]

FED-STD 209E — Airborne Particulate Cleanliness Classes in Clean Rooms and Clean Zones[7]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Available from Deutsches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, Website: www.din.de

6 Institute of Electrical and Electronics Engineers, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331, USA. Telephone: 732.981.0060; Fax: 732.981.1721

7 General Services Administration, Federal Supply Service, FSS Acquisition Management Center, Environmental Programs and Engineering Policy Division (FCOE), Washington, D.C. 20406 [Withdrawn from use in 2001, replaced by ISO 14644-1 and associated standards.]

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *ARAMS* — Automated Reliability, Availability, and Maintainability Standard

5.1.2 *ASCII* — American Standard Code for Information Interchange

5.1.3 *COP* — Crystal Originated Particle/Pit

5.1.4 *CRM* — Certified Reference Material

5.1.5 *FTP* —File Transfer Protocol

5.1.6 *GEM* — Generic Model for Communications and Control of Manufacturing Equipment

5.1.7 *HSMS* — High Speed SECS Message Services

5.1.8 *IEEE* — The Institute of Electrical and Electronic Engineers

5.1.9 *JPEG* — Joint Photographics Expert Group

5.1.10 *LLS* — Localized Light Scatterer

5.1.11 *LSE* — Latex Sphere Equivalent

5.1.12 *PSL spheres* — Polystyrene Latex spheres

5.1.13 *SECS II* — SEMI Equipment Communications Standard II

5.1.14 *SSIS* — Scanning Surface Inspection System

5.1.15 *XLS* — Extended Light Scatterer

5.1.16 *XML* — Extensible Markup Language

5.2 *Terminology Regarding Defect Type*

5.2.1 *COP (Crystal Originated Particle/Pit)* — A pit of approximately 100 nm in size bounded by crystallographic planes, and formed by the intersection of the polished surface with voids in the crystal.

5.2.1.1 *Discussion* — When the surface is cleaned, etched, or oxidized the shape of the pit is modified and the light scattering characteristics change. The spatial distribution of scattered light from COPs and particles is different, and therefore these two classes of defects may be distinguished by an appropriately equipped SSIS. COPs were first detected by SSIS and believed to be small particles. It was also noticed that after repeated cleaning (etching) the number of the COPs increased as the etching process enlarged the pits and changed their scattering characteristics. Later these defects were identified as voids caused by the coalescence of vacancies during the cooling of the silicon crystal from its growth temperature. The term crystal originated particle had already become accepted, and even today many people still refer to COPs by their original, though incorrect name.

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5.2.2 *dimple* — a shallow depression with gently sloping sides that exhibits a concave, spherical shape and is visible to the unaided eye under proper lighting conditions. [SEMI M1]

5.2.3 *haze* — non-localized light scattering resulting from surface topography (microroughness) or from dense concentrations of surface or near surface imperfections. [SEMI M1]

5.2.4 *mound (epitaxial wafer)* — regularly shaped bump on a semiconductor wafer surface, which may have one or more irregularly developed facets. [ASTM F 1241]

5.2.5 *mound (polished wafer)* — a defect characterized by small circular raised areas on the surface, typically 0.1 to 1.0 µm in height, 5 to 25 mm in diameter and located in random positions on the wafer.

5.2.6 *particle* — a small, discrete piece of foreign material or silicon not connected crystallographically to the wafer. [SEMI M1]

5.2.7 *pit* — a depression in a wafer surface that has steeply sloped sides that meet the surface in a distinguishable manner in contrast to the rounded sides of a dimple. [SEMATECH Technology Transfer 95082941A-TR]

5.2.8 *scratch* — a shallow groove or cut below the established plane of the wafer surface, with a length to width ratio greater than 5:1. [SEMATECH Technology Transfer 95082941A-TR

5.2.9 *slip* — a process of plastic deformation in which one part of a crystal undergoes a shear displacement relative to another in a fashion that preserves the crystallinity of the material. [ASTM F 1241]

5.2.10 *slurry ring* — a ring-shaped area, higher than the surrounding wafer surface caused by incomplete cleaning of slurry residue.

5.2.11 *spike* — in an epitaxial wafer, a tall thin dendrite of crystalline filament that often occurs at the center of a recess. [ASTM F 1241, see also ASTM F 154]

5.2.12 *stacking fault* — a two dimensional defect that results from a deviation from the normal stacking sequence of atoms in a crystal. [ASTM F 1241, see also ASTM F 154]

5.2.13 *stain* — area contamination that is chemical in nature and cannot be removed except through further lapping or polishing. [ASTM F 1241]

5.3 *Other Terminology*

5.3.1 *bias* — the difference between the average of measurements made on the same object and its true value. Sufficient measurements are needed to mitigate the effects of variability. [SEMI E89]

5.3.2 *calibration* — a measurement process that assigns a value to the property of an artifact or to the response of an instrument relative to reference standards or to a designated measurement process.

5.3.2.1 *Discussion* — The purpose of calibration is to eliminate or reduce bias in the user's measurement system relative to the reference base. The calibration process compares an unknown or test item or instrument with reference standards according to a specific algorithm, often in the form of a specific calibration curve. [SEMI E89]

5.3.3 *capture rate* — the probability that an SSIS detects an LLS of latex sphere equivalent (LSE) signal value at some specified SSIS operational setting.

5.3.4 *classification accuracy* — how many of a particular defect population are correctly classified.

5.3.4.1 *Discussion* — The accuracy of a classification system is expressed as an equation: Accuracy = A/H, where A is the total quantity of correctly classified defects (human and machine classification results agree) and H is the total quantity of human classified defects.

5.3.5 *classification purity* — how many of the defects classified by machine (SSIS) are properly classified.

5.3.5.1 *Discussion* — The purity of a classification system can be expressed as an equation: Purity = A/M, where A is the total quantity of correctly classified defects (human and machine classification results agree) and M is the total quantity of defects classified as a specific class by machine (SSIS).

5.3.6 *compatibility* — the capability of measurement equipment to emulate the measurement process of other tools. Downward compatibility refers to former generation(s) of the same or similar type of equipment of an equipment supplier.

5.3.7 *correlation* — the relation of measurement results obtained by repeated measurements with the same set of test specimen(s) and any two measurement tools expressed in terms of a regression curve.

5.3.8 *CRM (Certified Reference Material)* — reference material, accompanied by a certificate, one or more of whose property values are certified by a procedure which establishes its traceability to an accurate realization of the unit in which the property values are expressed, and for which each certified value is accompanied by an uncertainty at a stated level of confidence. [ISO Guide 30:1992]

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