SEMI M54-0304
GUIDE FOR SEMI-INSULATING (SI) GaAs MATERIAL PARAMETERS

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1 Purpose

1.1 Substrates with high electrical resistivity and electron drift mobility are needed to fabricate high performance digital and analog microelectronic devices and circuits. Semi-insulating *n*-type Gallium Arsenide, henceforth termed SI GaAs, has been established worldwide as a preferred substrate material for such applications.

1.2 The active layers needed for devices are generated either by ion implantation or by epitaxy. The quality of these layers, and hence the performance, yield and reliability of devices, strongly depends on the bulk and surface quality of the substrate.

1.3 This Document provides a basis for specifying the material parameters of SI GaAs to support ordering agreements between suppliers and purchasers.

2 Scope

2.1 This Document defines and describes the electrical, optical, structural, and surface properties of SI GaAs that are considered technically relevant according to the present status of scientific knowledge and material technology.

2.2 A specification of the material quality of SI GaAs substrates includes a number of the parameters described below. Depending on the intended application, a particular subset of properties and respective parameters will be considered relevant by the purchaser.

2.3 In order to enhance the clarity and applicability of the document, the ordering information in § 6 subdivides the material parameters in respect of their relative importance, according to general industry perception.

2.4 Some material properties and parameters, while intensively discussed in the technical literature, are insufficiently established to allow an unambiguous specification. The available information is nevertheless included to support supplier-purchaser discussions and agreements on these issues.

2.5 Each parameter specification requires an agreement about verification. Appropriate information is summarized in Section 5. Available standard test methods elaborated by SEMI, ASTM, and DIN are referenced in Section 3.

2.6 A number of the required standard test methods do not exist at present. This document is expected to serve as a guideline and incentive for qualified ASTM, DIN, JEITA, and SEMI committees to develop the missing standard procedures. Conversely, if at present more than one standard test method for verification of a specific parameter exists (see Table 1), a global consensus procedure towards selecting or generating a unique standard is advocated.

2.7 The geometrical properties of wafers, in particular orientation, diameter, thickness, flatness and edge rounding, are covered by the series of SEMI M9 specifications and shall not be addressed here.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M9 — Specifications for Polished Monocrystalline Gallium Arsenide Slices

SEMI M10 — Standard Nomenclature for Identification of Structures and Features Seen on Gallium Arsenide

SEMI M15 — Polished Wafer Defect Limits Table for Polished Gallium Arsenide Wafers

SEMI M30 — Standard Test Method for Substitutional Atomic Carbon Concentration in GaAs by Fourier Transform Infrared Absorption

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SEMI M36 — Test Method for Measuring Etch Pit Density (EPD) in Low Dislocation Density Gallium Arsenide Wafers

SEMI M39 — Test Method for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Semi-insulating GaAs Single Crystals

3.2 *ASTM Standards*[1]

ASTM F76 — Standard Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single-Crystal Semiconductors

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

3.3 *DIN Standards*[2]

DIN 50448 — Testing of Materials for Semiconductor Technology – Contactless Determination of the Electrical Resistivity of Semi-Insulation Semiconductor Slices Using a Capacitive Probe

DIN 50449-1 — Testing of Materials for Semiconductor Technology – Determination of Impurity Content in Semiconductors by Infrared Absorption – Part 1: Carbon in Gallium Arsenide

DIN 50449-2 — Testing of Materials for Semiconductor Technology – Determination of Impurity Content in Semiconductors by Infrared Absorption – Part 2: Boron in Gallium Arsenide

DIN 50454-1 — Testing of Materials for Semiconductor Technology – Determination of Dislocations in Monocrystals of III-V-Compound Semiconductors – Part 1: Gallium Arsenide

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 SI GaAs

4.1 SI GaAs as described in this specification has *n*-type conductivity and an electrical resistivity ρ in the range $1 \times 10^6 - 5 \times 10^8$ Ω·cm. It is characterized by fabrication procedures and material properties.

4.2 Synthesis of the compound GaAs from the elements gallium (Ga) and arsenic (As) may be done:

- in the crystal growth chamber immediately prior to growth (in-situ synthesis)
- in separate equipment, independent of crystal growth (ex-situ synthesis)

4.3 The growth of SI GaAs single crystals involves one of the following procedures:

- Liquid Encapsulated Czochralski (LEC)
- LEC with controlled As vapor pressure (VCZ)
- Vertical Gradient Freeze (VGF)
- Vertical Bridgman (VB)

4.4 SI GaAs single crystal ingots are thermally treated after crystal growth. The annealing procedures are defined by heating rates, hold temperatures, hold times and cooling rates. Single step ingot annealing (one hold time at one temperature) or multi step ingot annealing (several hold times at different temperatures) may be applied. Wafers may be treated similarly by single step wafer annealing and multi step wafer annealing.

4.5 SI GaAs contains the intrinsic double donor point defect EL2, which involves an As atom on a Ga site (As_{Ga}). At room temperature the first ionization level $EL2^0/EL2^+$ is approximately at $\Delta E = 0.69$ eV below the conduction band. The concentration $[EL2^0]$ of the neutral defect is in the range of 5×10^{15} to 3×10^{16} cm^{-3}.

[1] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, http://www.astm.org

[2] Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany; http://www.din.de

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4.6 SI GaAs contains unintentionally incorporated impurities acting as donors. It may also contain intrinsic donor defects other than EL2. The total concentration [D] of donors other than EL2 should be low for optimal control of ion implantation activation and high electron mobility μ (see ¶ 4.12).

4.7 SI GaAs contains impurities acting as acceptors. It may also contain intrinsic acceptor defects. Usually the total concentration [A] of acceptors is adjusted by controlled incorporation of carbon (C) in the concentration range [C] $4 \times 10^{14}\ cm^{-3} - 2 \times 10^{16}\ cm^{-3}$.

4.8 SI GaAs contains extrinsic and intrinsic point defects that do not participate in the compensation process (see §§ 4.10 and 4.11). These defects may be isoelectronic centers (e.g., boron (B) incorporated on the Ga site, B_{Ga}) or extremely deep donors and acceptors below and above the Fermi level, respectively. They may influence the material quality, for instance by degrading the activation efficiency of implanted dopants or by acting as transient carrier traps and nonradiative recombination centers (NRRC).

4.9 SI GaAs generally is nonstoichometric, containing excess As with a concentration of the order of $10^{18}\ cm^{-3}$. The excess As is partly incorporated as lattice antisite defects (As_{Ga}), see ¶ 4.5. Other forms of point defect incorporation (e.g., interstitial As) are likely, but have not been positively identified. Excess As is attracted by dislocations (see ¶ 4.13) and is concentrated along these, forming decoration precipitates. Precipitates may also be generated away from dislocations, e.g. in the inner part of dislocation cells (see ¶ 4.14). They are referred to as matrix precipitates and are generally smaller than dislocation precipitates. The concentration and size of precipitates strongly depend on the post growth annealing procedures (see ¶ 4.4).

4.10 To obtain SI GaAs, complete ionization of shallow donors and acceptors and partial single ionization of EL2 must be achieved, requiring that:

$$[EL2] > [A] - [D] > 0 \quad (1)$$

The Fermi level is then pinned approximately at ΔE below the conduction band.

4.11 The resistivity of SI GaAs is given by:

$$\rho = (e\,[n]\,\mu_n + e\,[p]\,\mu_p)^{-1} \quad (2a)$$

where e is the electron charge, [n] and [p] the concentration of electrons and holes and μ_n, μ_p the respective mobilities. For material with $\rho < 5 \times 10^8\ \Omega\cdot cm$ and meeting condition (1), the second term may be neglected, hence:

$$\rho = (e\,[n]\,\mu_n)^{-1} \quad (2b)$$

The electron concentration is given by:

$$[n] \propto [EL2^0] / [EL2^+] \exp(-\Delta E / kT) \quad (3)$$

where T is temperature, k is Boltzmann's constant and the concentration $[EL2^+]$ of the singly ionized defect is given by:

$$[EL2^+] = [A] - [D] \quad (4)$$

Equation 3 may be used to normalize resistivity data ρ_M taken at a measurement temperature T_M. The normalized resistivity ρ_S at a standard reference temperature T_S is calculated according to:

$$\rho_S = \rho_M \exp(\alpha\,\Delta T) \quad (5)$$

$$\text{where } \Delta T = T_M - T_S \quad (6)$$

and α depends on ΔE at T = 0 K (0.75 eV) and on T_S. For T_S = 296 K (23°C), one has α = 0.0994.

4.12 Due to ionized impurity scattering μ decreases with the concentration [I] of ionized centers, given by:

$$[I] = 2\,[A] = 2\,([EL2^+] + [D]) \quad (7)$$

Relations (3) and (7) imply that μ decreases with increasing resistivity. Relation (7) further implies that, for a given resistivity, low [D] is desirable to maximize μ.

4.13 SI GaAs ingots usually contain dislocations generated by thermal stress during crystal growth and postgrowth annealing. The dislocation density (DD), although a volume property, is evaluated by measuring the area density of dislocations threading a substrate surface. Structural etching with molten KOH generates characteristically shaped etch pits at the threading points. Hence the DD is characterized by quoting the etch pit density (EPD).

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