

SEMI M55-0304

SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON CARBIDE WAFERS

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NOTICE: The designation of SEMI M55 was updated during the 0304 publishing cycle to reflect the creation of SEMI M55.1.

1 Purpose

1.1 These specifications cover substrate requirements for monocrystalline high-purity silicon carbide wafers of crystallographic polytype 6H and 4H used in semiconductor and electronic device manufacturing.

2 Scope

2.1 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

2.2 These specifications are directed specifically to silicon carbide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.3 The material is Single Crystal Silicon Carbide (SiC) existing in many crystallographically different polytypes. For the most common polytypes the following properties in Table 1 are listed for use as guidelines:

Table 1 Common Properties¹

Polytype	4H	6H
Lattice Parameter		
a	3.076 Å	3.073 Å
c	10.053 Å	15.117 Å
Stacking Sequence	ABAC	ABCACB
Density	3.21 g/cm ³	3.21 g/cm ³
Melting Point	chemical decomposition above ca. 2800°C	chemical decomposition above ca. 2800°C
Dielectric Constant	9.7	9.7
Energy Gap	3.27 eV	3.02 eV

¹ Data as reported in Landolt-Börnstein (Springer Verlag)

2.4 For referee purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 SEMI Standards

SEMI M1 — Specification for Polished Monocrystalline Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

3.2 ASTM Standards²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With a Specified Tolerable Error, the Average for Characteristic of a Lot or Process

ASTM F26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

ASTM F154 — Standard Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

ASTM F523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

ASTM F533 — Standard Test Method for Thickness and Thickness Variation of Silicon Wafers

ASTM F534 — Standard Test Method for Bow of Silicon Wafers

ASTM F657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

² American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

ASTM F671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

ASTM F673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

ASTM F847 — Standard Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon and Wafers by X-Ray Techniques

ASTM F928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

ASTM F1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

ASTM F1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

ASTM F2074 — Standard Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.3 DIN Standards³

DIN 50441/1 — Measurement of the Geometric Dimensions of Semiconductor Wafers: Thickness and Thickness Variation

DIN 50448 — Testing of materials for semiconductor technology - Contactless determination of the electrical resistivity of semi-insulating semiconductor slices using a capacitive probe

3.4 JIS Standard⁴

JIS H 0611 — Methods of Measurement of Thickness Taper and Bow for Silicon Wafers

3.5 Other Standards

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes⁵

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M1, the SEMI Compilation of Terms, and ASTM F154.

4.1 Definitions

4.1.1 *bow* — of a semiconductor wafer, a measure of concave or convex deformation of the median surface of a wafer, independent of any thickness variation which may be present. Bow is a bulk property of the test specimen, not a property of an exposed surface. Generally, bow is determined with a test specimen in a free, unclamped condition. Units of bow are generally micrometers.

4.1.2 *crystallite* — any part of the wafer, having an arbitrary orientation of its crystallographic axis in respect to the monocrystalline part of the wafer.

4.1.3 *dopant* — a chemical element, usually from the third or fifth column of the periodic table for the case of IV-IV compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.4 *edge contouring* — on wafers whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the wafer joining the front and back sides.

4.1.5 *edge exclusion* — the width X of a narrow band of wafer surface, located just inside the wafer edge, over which the values of the specified parameter do not apply. See definition of *fixed quality area* below.

4.1.6 *fixed quality area (FQA)* — The central area of a wafer surface, defined by a nominal *edge exclusion*, X , over which the specified values of a parameter apply.

4.1.6.1 *Discussion* — The boundary of the FQA is at all points the distance X away from the periphery of a wafer of nominal dimensions. (See Figure 1.) The size of the FQA is independent of wafer diameter and flat length tolerances.

4.1.7 *lot* — for the purpose of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.8 *micropipe* — small hollow tube approximately parallel to the crystallographic c -axis and extending through the whole crystal.

³ Available from Deutsches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, website: www.din.de

⁴ Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp

⁵ American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202, USA

4.1.9 *orthogonal misorientation* — in {0001} wafers cut intentionally “off-orientation”, the angle between the projection of the vector normal to the wafer surface onto the {0001} plane and the projection on that plane of the specified direction of tilt in the {0001} plane. (See Figure 2.)

4.1.10 *planar defect* — small cavity in a SiC bulk crystal with large width-to-height ratio roughly parallel to the {0001} lattice plane. The lateral boundaries are parallel to crystallographic directions. Often one or more micropipes are connected to a planar defect.

4.1.11 *polytype* — one possible crystallographic modification of a substance which shows the phenomenon of polytypism. All polytypes of a substance have the same lattice layers with nearly the same lattice constant in common. However the stacking sequence of these layers differs between different polytypes. Most commonly polytypes are named after a suggestion of Ramsdell⁶: A symbol like 6H gives the number of layers in one periodic stacking sequence (2, 3, 4, ...) and the symmetry of the resulting crystal (H = hexagonal, R = rhombohedral). The most common polytypes of SiC are 6H, 4H, 15R.

4.1.12 *surface orientation* — the tilt angle between the crystallographic c-axis and the wafer surface normal. (See Figure 2.)

4.1.13 *total indicator reading (TIR)* — the smallest perpendicular distance between two planes, both parallel with the reference plane, which encloses all points on the front surface of a wafer within the FQA, the site, or the subsite, depending on which is specified.

4.1.14 *total thickness variation (TTV)* — the difference between the maximum and minimum thickness values of a wafer encountered during a scan pattern or a series of point requirements. TTV is generally expressed in micrometers.

4.1.15 *warp* — of a semiconductor slice or wafer, the difference between the maximum and minimum distance of the median surface of the wafer from a reference plane, encountered during a scan pattern. Warp is a bulk property of the test specimen, not a property of an exposed surface. Warp is generally expressed in micrometers.

5 Ordering Information

5.1 Purchase orders for silicon carbide wafers furnished to this specification shall include the following items:

5.1.1 Polytype,

5.1.2 Nominal diameter (see applicable SEMI Standard for polished SiC wafers),

5.1.3 Thickness (see applicable SEMI Standard for polished SiC wafers),

5.1.4 Dopant (see applicable SEMI Standard for polished SiC wafers),

5.1.5 Resistivity or Carrier Concentration (see applicable SEMI Standard for polished SiC wafers),

5.1.6 Total Thickness Variation (see applicable SEMI Standard for polished SiC wafers),

5.1.7 Surface orientation (see applicable SEMI Standard for polished SiC wafers),

5.1.8 Polarity of Surfaces (see applicable SEMI Standard for polished SiC wafers),

5.1.9 Lot Acceptance Procedures (see Section 7),

5.1.10 Certification (see Section 11), and

5.1.11 Packing and Marking (see Section 12).

6 Dimensions and Permissible Variations

6.1 The material shall conform to the dimensions and dimensional tolerances as specified in the applicable polished silicon carbide wafer standard.

6.2 The material shall conform to the crystallographic orientation details as specified in the applicable polished silicon carbide wafer standard.

6.3 If edge contoured wafers are specified on the purchase order, the profile shall conform to the following requirements at all points on the wafer periphery.

6.3.1 When the wafer is aligned with the SEMI Wafer Edge Profile Template (see Figure 3) so that the x-axis of the template is coincident with the wafer surface and the y-axis of the template forms a tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template. (See Figure 4 for example of acceptable and unacceptable contours.)

6.3.2 Cosmetic attributes of the edge contour are not covered by this specification. They shall be agreed upon between supplier and purchaser.

6.4 Flats shall conform to the requirements of Section 9 and the appropriate polished silicon carbide wafer standard.

NOTE 2: For edge chips and indents see Section 10.

⁶ L. S. Ramsdell, J. A. Kohn: Developments in Silicon Carbide Research, Acta Cryst. 5 (1952) 215 – 224