SEMI M55-0315
SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON CARBIDE WAFERS

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NOTICE: The designation of SEMI M55 was updated during the 0315 publishing cycle to reflect the revision of SEMI M55.4. No change was made to this Document.

1 Purpose

1.1 These specifications cover substrate requirements for monocrystalline high-purity silicon carbide wafers of crystallographic polytype 6H and 4H used in semiconductor and electronic device manufacturing.

2 Scope

2.1 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

2.2 These specifications are directed specifically to silicon carbide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.3 The material is Single Crystal Silicon Carbide (SiC) existing in many crystallographically different polytypes. For the most common polytypes the following properties in Table 1 are listed for use as guidelines:

Table 1 Common Properties[#1]

Polytype	*4H*	*6H*
Lattice Parameter a c	3.076 Å 10.053 Å	3.073 Å 15.117 Å
Stacking Sequence	ABAC	ABCACB
Density	3.21 g/cm^3	3.21 g/cm^3
Melting Point	chemical decomposition above ca. 2800°C	chemical decomposition above ca. 2800°C
Dielectric Constant	9.7	9.7
Energy Gap	3.27 eV	3.02 eV

#1 Data as reported in Landolt-Börnstein (Springer Verlag).

2.4 For reference purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

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SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

SEMI MF847 — Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon and Wafers by X-Ray Technologies

SEMI MF928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafer by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T5 — Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers

3.2 *ANSI Standard*[1]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standard*[2]

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With a Specified Tolerable Error, the Average for Characteristic of a Lot or Process

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

3.4 *DIN Standards*[3]

DIN 50441/1 — Measurement of the Geometric Dimensions of Semiconductor Wafers: Thickness and Thickness Variation

DIN 50448 — Testing of Materials for Semiconductor Technology – Contactless Determination of the Electrical Resistivity of Semi-Insulating Semiconductor Slices Using a Capacitive Probe

3.5 *JIS Standard*[4]

JIS H 0611 — Methods of Measurement of Thickness Taper and Bow for Silicon Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

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[1] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: 212.642.4900, Fax: 212.398.0023, http://www.ansi.org

[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: 610.832.9585, Fax: 610.832.9555, http://www.astm.org

[3] Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany; http://www.din.de

[4] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: 81.3.3583.8005, Fax: 81.3.3586.2014, http://www.jsa.or.jp

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4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M1, SEMI MF154, and the *SEMI International Standards: Compilation of Terms*.

4.1 *Definitions*

4.1.1 *bow* — of a semiconductor wafer, a measure of concave or convex deformation of the median surface of a wafer, independent of any thickness variation which may be present. Bow is a bulk property of the test specimen, not a property of an exposed surface. Generally, bow is determined with a test specimen in a free, unclamped condition. Units of bow are generally micrometers.

4.1.2 *crystallite* — any part of the wafer, having an arbitrary orientation of its crystallographic axis in respect to the monocrystalline part of the wafer.

4.1.3 *dopant* — a chemical element, usually from the third or fifth column of the periodic table for the case of IV-IV compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.4 *edge contouring* — on wafers whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the wafer joining the front and back sides.

4.1.5 *edge exclusion* — the width X of a narrow band of wafer surface, located just inside the wafer edge, over which the values of the specified parameter do not apply. See definition of *fixed quality area* below.

4.1.6 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal *edge exclusion*, *X*, over which the specified values of a parameter apply.

4.1.6.1 *Discussion* — The boundary of the FQA is at all points the distance *X* away from the periphery of a wafer of nominal dimensions (see Figure 1). The size of the FQA is independent of wafer diameter and flat length tolerances.

4.1.7 *lot* — for the purpose of this Document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.8 *micropipe* — small hollow tube approximately parallel to the crystallographic c-axis and extending through the whole crystal.

4.1.9 *orthogonal misorientation* — in {0001} wafers cut intentionally 'off-orientation', the angle between the projection of the vector normal to the wafer surface onto the {0001} plane and the projection on that plane of the specified direction of tilt in the {0001} plane (see Figure 2).

4.1.10 *planar defect* — small cavity in a SiC bulk crystal with large width-to-height ratio roughly parallel to the {0001} lattice plane. The lateral boundaries are parallel to crystallographic directions. Often one or more micropipes are connected to a planar defect.

4.1.11 *polytype* — one possible crystallographic modification of a substance which shows the phenomenon of polytypism. All polytypes of a substance have the same lattice layers with nearly the same lattice constant in common. However the stacking sequence of these layers differs between different polytypes. Most commonly polytypes are named after a suggestion of Ramsdell[5]: A symbol like 6H gives the number of layers in one periodic stacking sequence (2, 3, 4, ...) and the symmetry of the resulting crystal (H = hexagonal, R = rhombohedral). The most common polytypes of SiC are 6H, 4H, 15R.

4.1.12 *surface orientation* — the tilt angle between the crystallographic c-axis and the wafer surface normal (see Figure 2).

4.1.13 *total indicator reading (TIR)* — the smallest perpendicular distance between two planes, both parallel with the reference plane, which encloses all points on the front surface of a wafer within the FQA, the site, or the subsite, depending on which is specified.

4.1.14 *total thickness variation (TTV)* — the difference between the maximum and minimum thickness values of a wafer encountered during a scan pattern or a series of point requirements. TTV is generally expressed in micrometers.

[5] Ramsdell, L.S., Kohn, J. A. "Developments in Silicon Carbide Research." Acta Cryst. 5 (1952): pp. 215–24.

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