

SEMI M55-0921

SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON CARBIDE WAFERS

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and ¶¶) the symbols are used to reference more than one section or paragraph, respectively.

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1 Purpose

1.1 These specifications cover substrate requirements for monocrystalline high-purity silicon carbide wafers of crystallographic polytype 6H and 4H used in semiconductor and electronic device manufacturing.

2 Scope

2.1 A complete purchase specification may require the defining of additional physical, electrical, and bulk properties. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

2.2 These specifications are directed specifically to silicon carbide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.3 The material is Single Crystal Silicon Carbide (SiC) existing in many crystallographically different polytypes. For the most common polytypes the following properties in Table A1-1 are listed for use as guidelines.

2.4 This Standard addresses three main application areas for SiC substrates:

- High power applications (in this Document referred to as ‘HP’) employing homoepitaxy on conductive substrates
- High frequency applications (in this Document referred to as ‘HF’) employing heteroepitaxy on semi-insulating substrates
- Opto-electronic application (in this Document referred to as ‘OP’) employing heteroepitaxy on conductive substrates

2.5 For reference purposes, SI (System International, commonly called metric) units shall be used.

2.6 Dimensional requirements are provided for the following categories of polished wafers:

- 76.2 mm Round Polished Monocrystalline 4H and 6H Silicon Carbide Wafers
- 100.0 mm Round Polished Monocrystalline 4H and 6H Silicon Carbide Wafers
- 150.0 mm Round Polished Monocrystalline 4H and 6H Silicon Carbide Wafers
- 200.0 mm Round Polished Monocrystalline 4H and 6H Silicon Carbide Wafers

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI M81 — Guide to Defects Found on Monocrystalline Silicon Carbide Substrates

SEMI M83 — Test Method for Determination of Dislocation Etch Pit Density in Monocrystals of III-V Compound Semiconductors

SEMI M87 — Test Method for Contactless Resistivity Measurement of Semi-Insulating Semiconductors

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafer by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T5 — Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers

3.2 *ASTM Standards*¹

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With a Specified Tolerable Error, the Average for Characteristic of a Lot or Process

3.3 *ASQ Standards*²

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M81 and SEMI MF154.

4.1 *Abbreviations and Acronyms*

4.1.1 *HF* — high frequency

4.1.2 *HP* — high power

4.1.3 *OP* — opto-electronic

4.2 *Definitions*

4.2.1 *crystallite* — any part of the wafer, having an arbitrary orientation of its crystallographic axis in respect to the monocrystalline part of the wafer.

4.2.2 *dopant* — a chemical element, usually from the third or fifth column of the periodic table for the case of IV-IV compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.2.3 *edge contouring* — on wafers whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the wafer joining the front and back sides.

4.2.4 *edge exclusion (EE)* — the distance from the FQA boundary to periphery of a wafer of nominal dimensions. See definition of fixed quality area below.

4.2.5 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal edge exclusion, EE over which the specified values of a parameter apply. Because the nominal edge exclusion relates to the nominal diameter of a wafer, the size of the FQA is independent of wafer diameter and flat length tolerances.

4.2.6 *high frequency (HF)* — applications employing heteroepitaxy on semi-insulating SiC substrates.

4.2.7 *high power (HP)* — applications employing homoepitaxy on conductive SiC substrates.

¹ ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>

² American Society for Quality, 600 North Plankinton Avenue, Milwaukee, WI 53203, USA; Telephone: +1.414.272.8575, Fax: +1.414.272.1734, <http://www.asq.org>

4.2.8 *GBIR* — flatness property, see SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as ‘total thickness variation (TTV)’.

4.2.9 *GMLYMER* — flatness property, see SEMI M1, Appendix 3, Shape Decision Tree. Formerly also known as ‘Warp’.

4.2.10 *lot* — for the purpose of this Document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.2.11 *micropipe* — small hollow tube basically parallel to the crystallographic c-axis and extending typically through larger parts of the crystal boule and thus affecting several neighboring wafers. Micropipes may be generated at bulk defects e.g. inclusions, polytype defects or crystallites. (See SEMI M81 for examples.)

4.2.12 *off-orientation* — the tilt angle between the crystallographic c-axis and the wafer surface normal (see Figure A2-2).

4.2.13 *opto-electronic (OP)* — application employing heteroepitaxy on conductive SiC substrates.

4.2.14 *orthogonal misorientation* — in {0001} wafers cut intentionally ‘off-orientation’, the angle between the projection of the vector normal to the wafer surface onto the {0001} plane and the projection on that plane of the specified direction of tilt in the {0001} plane (see Figure A2-2).

4.2.15 *planar defect* — small cavity in a SiC bulk crystal with large width-to-height ratio roughly parallel to the {0001} lattice plane. The lateral boundaries are parallel to crystallographic directions. Often one or more micropipes are connected to a planar defect. (See SEMI M81 for examples.)

4.2.16 *polytype* — one possible crystallographic modification of a substance which shows the phenomenon of polytypism. All polytypes of a substance have the same lattice layers with nearly the same lattice constant in common. However the stacking sequence of these layers differs between different polytypes. Most commonly polytypes are named after a suggestion of Ramsdell³: A symbol like 6H gives the number of layers in one periodic stacking sequence (2, 3, 4, ...) and the symmetry of the resulting crystal (H = hexagonal, R = rhombohedral, C = cubic). The most common polytypes of SiC are 6H, 4H, 15R, 3C.

4.2.17 *SBIR* — flatness property, see SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as ‘local thickness variation (LTV or LTVmax)’.

4.2.18 *SFQR* — flatness property, see SEMI M1, Appendix 1, Flatness Decision Tree.

4.2.19 *total thickness variation (TTV)* — see GBIR.

4.2.20 *warp* — see GMLYMER.

5 Ordering Information

5.1 Purchase orders for silicon carbide wafers furnished to this Specification shall include the following items (see Table A1-12 for a list of possible specifications):

- Polytype,
- Dopant and Conductivity Type (see Table A1-10),
- Nominal Diameter (see Tables A1-6, A1-7, A1-8, and A1-9),
- Thickness (see Tables A1-6, A1-7, A1-8, and A1-9),
- Primary Flat Length (only 150 mm diameter, see Table A1-8),
- Polarity of the Front (Device) Surface,
- Surface Orientation (see Table A1-11),
- Primary Flat Orientation Tolerance (only 100 mm and 150 mm diameter, see Table A1-11),

³ Ramsdell, L. S., Kohn, J. A. “Developments in Silicon Carbide Research.” Acta Cryst. 5 (1952): pp. 215–224.

- Orthogonal Misorientation Tolerance (only 100 mm and 150 mm diameter, see Table A1-11),
- Edge Shape Template (see Tables A1-6, A1-7, A1-8, and A1-9),
- Resistivity (see Table A1-2),
- Etch Pit Density,
- Micropipe Density,
- Lot Acceptance Procedures (see § 8),
- Certification (see § 9), and
- Packing and Marking (see § 10).

6 Requirements

6.1 General Characteristics

6.1.1 The crystal growth method shall be agreed upon by customer and supplier.

6.2 Electrical Characteristics

6.2.1 Electrical requirements are shown in Table A1-2.

6.3 Structural Characteristics

6.3.1 Standard Defect Limits

6.3.1.1 The material shall conform to the crystallographic orientation details as specified in Table A1-11.

6.3.1.2 Flats and notches shall conform to the requirements of § 6.4.1.

6.3.2 Surface Defects

6.3.2.1 The material shall conform to the requirements of Table A1-4 (see also Figure A2-3).

6.3.2.2 Minimal conditions or dimensions for surface defects are stated below. These limits shall be used for determining wafer acceptability; anomalies smaller than these limits shall not be considered as defects.

6.3.2.3 Surface Defect Definitions

6.3.2.3.1 *Edge Chip and Indent* — Any edge anomaly including saw exit marks conforming to the definition [SEMI MF154] and greater than 0.25 mm in radial depth and peripheral length.

6.3.2.3.2 *Orange Peel* — Any visually detectable roughened surface conforming to the definition [SEMI MF154] and observable under diffused illumination. Pits with a spacing of less than 2 mm are also treated as orange peel.

6.3.2.3.3 *Particles* — Distinct particles resting on the surface which are revealed under collimated intense light as bright points.

6.3.2.3.4 *Pit* — Any individually distinguishable depression in the surface with a length-to-width ratio smaller than 5:1, visible when viewed under intense illumination.

6.3.2.3.4.1 *Discussion* — This definition is different from SEMI MF154 in so far as the slope of the sides of the depression are not taken into account.

6.3.2.3.5 *Scratch* — Any anomaly conforming to the definition [SEMI MF154] and having a length-to-width ratio greater than 5:1 and visible under intense illumination.

6.3.3 Bulk Defects

6.3.3.1 The material shall conform to the requirements of Table A1-4 (see also Figure A2-3).

6.3.3.2 Bulk Defect Definitions

6.3.3.2.1 *Crack* — Any anomaly conforming to the definition [SEMI MF154] and greater than 0.25 mm in total length.

6.3.3.2.2 *Crystallite* — Any anomaly conforming to the definition (see § 4.2.1) and having a misorientation of more than 1° to the main (monocrystalline) part of the wafer and having a maximum width larger than 0.20 mm.

6.3.3.2.3 *Micropipe* — Any anomaly conforming to the definition (see § 4.2.11) and visible by microscopic inspection in transmission mode at a magnification of 100× or after etching in molten KOH, which will reveal micropipes as hexagonal structures. (See also SEMI M81.)

6.3.3.2.3.1 *Discussion* — For microscopic inspection the use of crossed polarizers is recommended. However not all micropipes will be visible under crossed polarizers.

6.3.3.2.4 *Planar Defect* — Any anomaly conforming to the definition (see § 4.2.15) having a maximum width larger than 0.20 mm.

6.4 Wafer Preparation Characteristics

6.4.1 Wafer Flat System

6.4.1.1 For silicon carbide wafers up to 150 mm diameter with the surface normal close to the crystallographic *c*-axis (small tilt angles, see Figure A2-2) one primary orientation flat and depending on the application and diameter one secondary flat is specified. For high-frequency applications a notch replacing the primary flat may also be specified. The primary flat always has a greater flat length compared to the secondary flat, if present (see Figure A2-4). For silicon carbide wafers with 200 mm diameter a notch is specified.

6.4.1.2 The angle between primary and secondary flat is always 90° (see Figure A2-5). For the tolerance see Table A1-11.

6.4.1.3 The polarity of the wafer surfaces is indicated by the relative flat positions of primary and secondary flat as shown in Figure A2-5. In the case of no secondary flat or of a notch the laser mark on the backside indicates the polarity.

6.4.1.4 The edge of the primary flat is always parallel to the [11-20] direction (or, equivalently, parallel to the (1-100) lattice plane) (see Figure A2-5), the line from wafer center to the notch is always parallel to the [1-100] direction (see Figure A2-6), respectively. For tolerances see the Table A1-11.

6.4.1.5 For the exact dimensions of the flat length and the tolerances see Table A1-6, Table A1-7, or Table A1-8 respectively. Notch dimensions are specified in Figure A2-11.

6.4.2 Wafer ID Marking

6.4.2.1 The wafers supplied under these specifications shall be identified by an individual laser marking consisting of the supplier assigned lot-number on the backside of each wafer. See SEMI T5 for the standard criteria for alphanumeric marking of SiC wafers.

6.4.3 Edge Contouring

6.4.3.1 If edge contoured wafers are specified on the purchase order, the profile shall conform to the following requirements at all points on the wafer periphery and given by Table A1-5.

6.4.3.2 When the wafer is aligned with the SEMI Wafer Edge Profile Template (see Figure A2-7) so that the *x*-axis of the template is coincident with the wafer surface and the *y*-axis of the template forms a tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template (see Figure A2-8 for example of acceptable and unacceptable contours).

6.4.3.3 Cosmetic attributes of the edge contour are not covered by this Specification. They shall be agreed upon between supplier and purchaser.

6.5 *Dimensional Characteristics* — See Tables A1-6, A1-7, A1-8, and A1-9.

7 Sampling

7.1 Unless otherwise specified, ASTM E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQ Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these