SEMI M57-0305
GUIDE FOR SPECIFYING SILICON ANNEALED WAFERS

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on December 10, 2004. Initially available at www.semi.org in February 2005; to be published March 2005. Originally published July 2004.

NOTICE: This document was completely rewritten in March 2005.

1 Purpose

1.1 A number of device manufacturers utilize silicon annealed wafers to gain improved device characteristics. This guide provides information for developing specifications for silicon annealed wafers used to fabricate semiconductor devices and integrated circuits.

2 Scope

2.1 This guide covers dimensional, electrical, chemical, and structural properties of silicon annealed wafers for 180 nm, 130 nm, and 90 nm device technology generations.

2.2 Based on the guidance herein, the user of the guide can generate specifications for silicon annealed wafers.

2.3 One of the reasons for using annealed wafers is to allow a reduction in the crystal originated particles (COP) near the top surface region of the wafer. Currently, only the COP surface density can be estimated.

2.4 The width of the denuded zone (DZ) free of bulk micro defects (BMD) is also an important parameter. However, there is no standardized method to evaluate this characteristic at the present time.

2.5 The complete EDI Code List for items in the Order Form appropriate to silicon wafers, including annealed wafers, can be found in SEMI M18.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M45 — Provisional Specification for 300 mm Wafer Shipping System

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF391 — Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

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SEMI MF951 — Test Method for Determination if Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF1239 — Test Methods for Oxygen Precipitation Characteristics of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *JIS Standards*[1]

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

Z 8741 — Specular Glossiness–Method of Measurement

3.3 *DIN Standards*[2]

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

50443/1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-Ray Topography: Silicon

3.4 *ISO Standard*[3]

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence Spectroscopy (TXRF) on silicon wafers by total reflection X-ray fluorescence spectroscopy (TXRF)

3.5 *ANSI Standards*[4]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/EIA 556-B — Outer Shipping Container Standard

3.6 *ASTM Standards*[5]

D 523 — Standard Test Method for Specular Gloss

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

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1 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp.

2 Deutches Institut für Normung e.V., standards are available in both English and German editions from Beuth Verlag GmbH, Burggrafenstrasse 6, 10787 Berlin, Germany, Telephone: 49.30.2601-0, Fax: 49.30.2601.1263, Website: www.beuth.de

3 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch.

4 American National Standards Institute, New York Office: 25 West 43rd Street, New York, NY 10036, USA. Telephone: 212.642.4900, Fax: 212.398.0023, Website: www.ansi.org

5 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555, Website: www.astm.org

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4 Terminology

4.1 Most general terms, acronyms, and symbols relating to silicon technology are defined in SEMI M59.

4.2 Terms specific to commonly-used annealed wafers are defined as follows:

4.2.1 *annealed wafer* — wafer that has a defect (COP) free zone near the surface resulting from high temperature annealing under a neutral or reducing atmosphere.

4.2.2 *argon annealed wafer* — annealed wafer produced under argon atmosphere.

4.2.3 *hydrogen annealed wafer* — annealed wafer produced under hydrogen atmosphere.

5 Ordering Information

5.1 Purchase orders for silicon annealed wafers furnished to this guide shall include the appropriate order entry information from Table 1, Polished Wafer Specification Format for Order Entry, in SEMI M1. All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included:

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.6 Nominal Edge Exclusion
- 2-1.7 Co-dopant in Crystal
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity (Center point)
- 2-2.2 Radial Resistivity Variation
- 2-3.1 Oxygen Concentration/Calibration Factor
- 2-3.2 Radial Oxygen Variation
- 2-3.3 Carbon Concentration (Background)
- 2-4.3 Lineage
- 2-4.4 Twin Boundary
- 2-4.5 Swirl
- 2-5.1 Wafer ID Marking
- 2-5.2 Front Surface Thin Films
- 2-5.4 Extrinsic Gettering
- 2-5.5 Backseal
- 2-6.1 Diameter
- 2-6.6 Edge Profile
- 2-6.7 Thickness
- 2-6.8 Total Thickness Variation (TTV)
- 2-9.1 Edge Chips (Back Surface)
- 2-9.8 Brightness (Gloss) (Back Surface)
- 2-9.9 Scratches (Macro) (Back Surface)

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Table 1 Silicon Wafer Specification Format for Order Entry, Part 5 Annealed Wafers

ITEM			*SPECIFICATION*	*MEASUREMENT METHOD*
5-1. ANNEALING CONDITIONS				
	5-1.1	Annealing Atmosphere	[ ]Hydrogen; [ ]Argon; [ ]Other: (specify)_____	
5-2. POST-ANNEAL WAFER PREPARATION CHARACTERISTIC				
	5-2.1	Edge Surface Condition	[ ]Ground; [ ]Etched; [ ]Polished[A]	
5-3. POST-ANNEAL DIMENSIONAL CHARACTERISTICS				
	5-3.1	Warp	[ ] µm; max.	[ ]SEMI MF657; [ ]SEMI MF1390; [ ]Other: (specify)_____
	5-3.2	Flatness, Site	Acronym[#2]: [ ] [ ] [ ] [ ] Value: Not greater than [ ]µm Site Size ___ mm × ___ mm % Usable Area_____ [ ]Include partial sites; [ ]Do not include partial sites Offset: x = [ ] mm, y = [ ] mm	[ ]SEMI MF1530; [ ]Other: (specify)_____
5-4. POST-ANNEAL FRONT SURFACE CHEMISTRY				
	5-4.1	Surface Metal Contamination		
	5-4.1.1	Sodium	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	5-4.1.2	Aluminum	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	5-4.1.3	Potassium	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF);[ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.4	Chromium	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF);[ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.5	Iron	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF);[ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.6	Nickel	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF);[ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.7	Copper	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF);[ ]ISO 14706 (TXRF); [ ]Other: (specify)_____

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