SEMI M57-0414
SPECIFICATIONS FOR SILICON ANNEALED WAFERS

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1 Purpose

1.1 A number of device manufacturers utilize silicon annealed wafers to gain improved device characteristics. These specifications provide information for developing specifications for silicon annealed wafers used to fabricate semiconductor devices and integrated circuits.

2 Scope

2.1 These specifications cover dimensional, electrical, chemical, and structural properties of silicon annealed wafers for 180 nm, 130 nm, 90 nm, (Table R1-1), 65 nm, 45 nm, 32 nm, (Table R1-2), and 22 nm (Table R1-3) device technology generations.

2.2 Based on the guidance herein, the user of this Document can generate specifications for silicon annealed wafers.

2.3 One of the reasons for using annealed wafers is to allow a reduction in the crystal originated pits (COP), also sometimes known as crystal originated particles, near the top surface region of the wafer. The width of the denuded zone (DZ) free of bulk micro defects (BMD) is also an important parameter.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF391 — Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF951 — Test Method for Determination if Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF1239 — Test Methods for Oxygen Precipitation Characteristics of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

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SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI Standards*[1]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/EIA 556-B — Outer Shipping Container Bar Code Label Standard

3.3 *ASTM Standards*[2]

ASTM D523 — Standard Test Method for Specular Gloss

ASTM E122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

3.4 *ISO Standard*[3]

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence Spectroscopy (TXRF) on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy (TXRF)

3.5 *JEITA Standards*[4]

JEITA EM-3508 — Test Method for Bulk Micro Defect Density and Denuded Zone Width in Annealed Silicon Wafers

JEITA EM-3509 — Sample Preparation Method for Minority Carrier Diffusion Length Measurement in Silicon Wafers by Surface Photovoltage Method

3.6 *JIS Standards*[5]

JIS H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

JIS Z 8741 — Specular Glossiness–Method of Measurement

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Most general terms, acronyms, and symbols relating to silicon technology are defined in SEMI M59.

4.2 Terms specific to commonly-used annealed wafers are defined as follows:

4.2.1 *annealed wafer* — wafer that has a defect (COP) free zone near the surface resulting from high temperature annealing under a neutral or reducing atmosphere.

[1] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: 212.642.4900, Fax: 212.398.0023, http://www.ansi.org

[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: 610.832.9585, Fax: 610.832.9555, http://www.astm.org

[3] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, http://www.iso.ch

[4] Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; http://www.jeita.or.jp

[5] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: 81.3.3583.8005, Fax: 81.3.3586.2014, http://www.jsa.or.jp

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4.2.2 *argon annealed wafer* — annealed wafer produced under argon atmosphere.

4.2.3 *hydrogen annealed wafer* — annealed wafer produced under hydrogen atmosphere.

5 Ordering Information

5.1 Purchase orders for silicon annealed wafers furnished to these specifications shall include the appropriate order entry information from Table 1, Polished Wafer Specification Format for Order Entry, in SEMI M1. All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included:

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.6 Nominal Edge Exclusion
- 2-1.7 Co-dopant in Crystal
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity (Center point)
- 2-2.2 Radial Resistivity Variation
- 2-3.1 Oxygen Concentration/Calibration Factor
- 2-3.2 Radial Oxygen Variation
- 2-3.3 Carbon Concentration (Background)
- 2-4.3 Lineage
- 2-4.4 Twin Boundary
- 2-4.5 Swirl
- 2-5.1 Wafer ID Marking
- 2-5.2 Front Surface Thin Films
- 2-5.4 Extrinsic Gettering
- 2-5.5 Backseal
- 2-6.1 Diameter
- 2-6.6 Edge Profile
- 2-6.7 Thickness
- 2-6.8 Total Thickness Variation (TTV)
- 2-8.6 Edge Chips
- 2-9.1 Edge Chips (Back Surface)
- 2-9.8 Brightness (Gloss) (Back Surface)
- 2-9.9 Scratches (Macro) (Back Surface)

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Table 1 Silicon Wafer Specification Format for Order Entry, Part 5 Annealed Wafers

ITEM		*SPECIFICATION*	*MEASUREMENT METHOD*
5-1. ANNEALING CONDITIONS			
5-1.1	Annealing Atmosphere	[ ] Hydrogen; [ ] Argon; [ ] Other: (specify)_____	
5-2. POST-ANNEAL WAFER PREPARATION CHARACTERISTIC			
5-2.1	Edge Surface Condition	[ ] Ground; [ ] Etched; [ ] Polished[A]	
5-3. POST-ANNEAL DIMENSIONAL CHARACTERISTICS			
5-3.1	Warp	[ ] µm; max.	[ ] SEMI MF657; [ ] SEMI MF1390; [ ] Other: (specify)_____
5-3.2	Flatness, Site	Acronym[#2]: [ ] [ ] [ ] [ ] Value: Not greater than [ ]µm Site Size ___ mm × ___ mm % Usable Area_____ [ ]Include partial sites; [ ]Do not include partial sites Offset: x = [ ] mm, y = [ ] mm	[ ] SEMI MF1530; [ ] Other: (specify)_____
5-4. POST-ANNEAL FRONT SURFACE CHEMISTRY			
5-4.1	Surface Metal Contamination		
5-4.1.1	Sodium	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] Other: (specify)_____
5-4.1.2	Aluminum	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] Other: (specify)_____
5-4.1.3	Potassium	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
5-4.1.4	Chromium	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
5-4.1.5	Iron	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
5-4.1.6	Nickel	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
5-4.1.7	Copper	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
5-4.1.8	Zinc	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____

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ITEM		SPECIFICATION	MEASUREMENT METHOD
5-4.2	**Other Surface Metals (List Separately)**		
5-4.2.1	Calcium	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
5-5. POST-ANNEAL FRONT SURFACE INSPECTION CHARACTERISTICS			
5-5.1	Slip	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
5-5.2	Oxidation Induced Stacking Faults (OSF)	[ ] None; [ ] Not greater than [ ] per cm^2	Test Cycle: [ ] SEMI MF1727; [ ] JIS H 0609; [ ] Other: (specify)_____ Observation Method: [ ] SEMI MF1726; [ ] JIS H 0609; [ ] Other: (specify)_____
5-5.3	Scratches – Macro	[ ] None; Total Length = [ ] mm	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#3] [ ] Other: (specify)_____
5-5.4	Scratches – Micro	[ ] None; [ ] Total Length = [ ] mm	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#3] [ ] Other: (specify)_____
5-5.5	Haze	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#3] [ ] Other: (specify)_____
5-5.6	Localized Light Scatterers (Total LLS)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#3] [ ] Other: (specify)_____
5-5.7	Localized Light Scatterers (COP only)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#3] [ ] Other: (specify)_____
5-5.8	Other Front Surface Defects	Terracing, Surface microroughness, Nanotopography, and other attributes as discussed between supplier and customer	As discussed between supplier and customer.
5-6. POST- ANNEAL BACK SURFACE INSPECTION CHARACTERISTICS			
5-6.1	Contamination/Area	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
5-6.2	Other Back Surface Defects	Support-related back surface defects as discussed between supplier and customer	As discussed between supplier and customer.
5-7. OTHER POST-ANNEAL CHARACTERISTICS			
5-7.1	Bulk Iron (Fe)	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^3	[ ] SEMI MF391; [ ] SEMI MF1535; [ ] JEITA EM-3509; [ ] Other: (specify)_____
5-7.2	Depth of BMD Denuded Zone	[ ] more than [ ] µm	Test Cycle: SEMI MF1239 [ ]A, [ ]B; Other: (specify)_____ Determination of DZ Depth [ ] JEITA EM-3508; [ ] Other: (specify)_____
5-7.3	BMD Density	Range [ ] × $10^{[\ ]}$ to [ ] × $10^{[\ ]}$ Unit Unit: [ ]cm^{-2}; [ ]cm^{-3}	Test Cycle: SEMI MF1239 [ ]A, [ ]B; Other: (specify)_____ Determination of BMD Density [ ] JEITA EM-3508; [ ] Other: (specify)_____

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