

SEMI M59-1105

TERMINOLOGY FOR SILICON TECHNOLOGY

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1 Purpose

1.1 Silicon technology underlies the integrated circuit and device industry. To promote common understanding and correct communication between suppliers and customers and others in the field, terms used in this field should be defined.

1.2 This terminology document covers definitions of terms used in relation to semiconductor silicon crystals and wafers.

2 Scope

2.1 This terminology covers terms describing attributes of silicon wafers as specified in SEMI M1 and other SEMI standards as outlined in SEMI M1. These attributes include electrical, structural, chemical, and dimensional characteristics of polished and other types of silicon wafers as well as surface defects and contamination.

2.2 This terminology is applicable for use in connection with research, development, process control, inspection, and procurement of silicon material.

2.3 Almost all of the terms for which definitions are listed are nouns. Unless the part of speech is given for any particular term, it can be assumed that the term is a noun.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI MF1811 — Practice for Estimating the Power Spectral Density Function and Related Finish Parameters from Surface Profile Data

3.2 ISO Standard¹

ISO 4287/1 — Surface Roughness – Terminology – Part 1: Surface and its Parameters

3.3 ANSI Standard²

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Abbreviations and Acronyms

4.1 AAS — atomic absorption spectroscopy, a method for analyzing for impurities.

4.2 AFM — atomic force microscope, an instrument for measuring microroughness.

4.3 A/N — alphanumeric.

¹ International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembe, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch.

² American National Standards Institute, New York Office: 25 West 43rd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org.

- 4.4 *ANSI* — American National Standards Institute², the American member of ISO.
- 4.5 *As* — arsenic, an *n*-type dopant in silicon.
- 4.6 *ASTM* — ASTM International,³ previously the American Society for Testing and Materials, an American organization that developed standards for silicon technology between 1964 and 2002; these standards, though developed primarily by American experts have been used world-wide.
- 4.7 *B* — boron, a *p*-type dopant in silicon.
- 4.8 *BMD* — bulk micro defect.
- 4.9 *BRDF* — bi-directional reflectance distribution function.
- 4.10 *CCW* — counterclockwise, rotation in the direction opposite to that of the hands of a clock.
- 4.11 *COP* — crystal originated pit, a small pit or plurality of small pits introduced during crystal growth that act as an LLS.
- 4.12 *CRM* — certified reference material.
- 4.13 *CVD* — chemical vapor deposition, a method for producing epitaxial films.
- 4.14 *CW* — clockwise, rotation in the direction of the hands of a clock.
- 4.15 *Cz* — Czochralski, a type of crystal growth.
- 4.16 *DDS* — difference data set, the difference between the reference data set and the sample data set.
- 4.17 *DI* — deionized, generally referred to in connection with electronic grade water.
- 4.18 *DIN* — Deutsches Institut für Normung,⁴ the German national standards organization, which has developed numerous standards for silicon during the last three decades.
- 4.19 *FPD* — focal plane deviation.
- 4.20 *FQA* — fixed quality area of a silicon wafer.
- 4.21 *FZ* — float zone, a type of crystal growth.
- 4.22 *GBIR* — the most common type of global flatness, see Appendix 1 of SEMI M1 for other types of global flatness.
- 4.23 *GFA* — gas fusion analysis, a method for measuring total oxygen in silicon.
- 4.24 *GRR* — grand round robin, the international interlaboratory experiment that established IOC-88.
- 4.25 *IC* — integrated circuit.
- 4.26 *ICP/MS* — inductively coupled plasma mass spectroscopy, a method for analysis of impurities, not yet standardized.
- 4.27 *IOC-88* — international oxygen conversion factor-1988, the currently universally adopted conversion factor between the infrared absorption peak and the interstitial oxygen content in silicon.
- 4.28 *ID* — identification, referring to the laser mark on silicon and other semiconductor wafers.
- 4.29 *ISO* — International Organization for Standardization,¹ a body recognized by the World Trade Organization as a developer of international standards, including a few applicable to silicon technology.
- 4.30 *JEIDA* — Japan Electronic Industry Development Association, now JEITA
- 4.31 *JEITA* — Japanese Electronic and Information Technology Industries Association,⁵ successor to JEIDA upon the merging of JEIDA and the Electronic Industries Association of Japan (EIAJ), which has a committee that develops standards for silicon materials and technology.

3 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org.

4 Deutsches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D 10787 Berlin, Germany, website: www.din.de.

- 4.32 *JIS* — Japan Industrial Standard, standards published by the Japanese Standards Association.⁶
- 4.33 *LLS* — localized light scatterer.
- 4.34 *LPD* — light point defect, a term formerly widely used, but now superseded by the term *LLS*.
- 4.35 *MAE* — mixed acid etchant.
- 4.36 *MCz* — magnetic Czochralski, a type of crystal growth that generally yields crystals with lower oxygen content than *Cz* growth.
- 4.37 *NTD* — neutron transmutation doped, a method for forming high resistivity *n*-type silicon.
- 4.38 *OSF* — oxidation induced stacking fault, a defect in silicon wafers.
- 4.39 *P* — phosphorus, an *n*-type dopant in silicon.
- 4.40 *ppba* — parts per billion atomic.
- 4.41 *ppbw* — parts per billion by weight.
- 4.42 *ppma* — parts per million atomic.
- 4.43 *ppmw* — parts per million by weight.
- 4.44 *PSD* — power spectral density.
- 4.45 *PTFE* — polytetrafluoroethylene, an HF-resistant material for sample bottles, lids, and tongs.
- 4.46 *RDS* — reference data set.
- 4.47 *rf* — radio frequency.
- 4.48 *RPD* — reference plane deviation.
- 4.49 *RSF* — relative sensitivity factor, used in TXRF analysis of surface metals to relate the concentrations of a variety of elements to the calibration element.
- 4.50 *Sb* — antimony, an *n*-type dopant in silicon.
- 4.51 *SCFM* — standard cubic feet per minute.
- 4.52 *SDS* — sample data set.
- 4.53 *SFQR* — the most commonly used type of site flatness, see Appendix 1 of SEMI M1 for other types of site flatness.
- 4.54 *Si* — silicon.
- 4.55 *SIMS* — secondary ion mass spectroscopy, a method for analysis of impurities.
- 4.56 *SPC* — statistical process control.
- 4.57 *SRM* — registered trademark for a CRM produced by the National Institute for Standards and Technology.
- 4.58 *SSIS* — scanning surface inspection system.
- 4.59 *TIR* — total indicator reading (also known as total indicator runout).
- 4.60 *TTV* — total thickness variation.
- 4.61 *TXRF* — total reflection x-ray reflectance spectroscopy, a surface metal analysis technique.
- 4.62 *VPD* — vapor phase decomposition, a method for dissolving an oxide film containing impurities to be examined by means of hydrofluoric (HF) acid vapor.

⁵ Japan Electronics and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan, Website: www.jeita.or.jp.

⁶ Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp.

4.63 *XLS* — extended light scatterer.

5 Definitions

5.1 *acceptor* — an impurity in a semiconductor that accepts electrons excited from the valence band, leading to hole conduction.

5.2 *anisotropic, adj.* — exhibiting different physical properties in differing crystallographic directions.

5.3 *anisotropic etch* — a selective etch that exhibits an accelerated etch rate along specific crystallographic directions.

5.3.1 *Discussion* — Anisotropic etches are used to determine crystal orientation, to fabricate micromechanical structures, and to facilitate dielectric component isolation.

5.4 *annealed wafer* — wafer that has a defect (COP) free zone near the surface resulting from high temperature annealing under a neutral or reducing atmosphere.

5.5 *annealing* — a high temperature process that alters the characteristics of the wafer.

5.6 *autodoping, of an epitaxial layer* — incorporation of dopant originating from the substrate into the epitaxial layer. Also called *self-doping*.

5.6.1 *Discussion* — Sources of autodoping can be the back and front surfaces and edges of the substrate, other substrates in the reactor, the susceptor, or other parts of the deposition assembly.

5.7 *back surface* — the exposed surface opposite to that upon which active semiconductor devices have been or will be fabricated.

5.8 *backseal* — a film of silicon dioxide or other insulator placed over the back surface of a silicon wafer to inhibit outdiffusion of the majority dopant impurity.

5.9 *backside* — not preferred, use *back surface*.

5.10 *bow* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer.

5.11 *carrier* — an entity capable of carrying electric charge through a solid, for example, valence holes and conduction electrons in semiconductors; also known as *charge carrier*.

5.12 *chemical vapor deposition (CVD), in semiconductor technology* — a process in which a controlled chemical reaction produces a thin surface film.

5.12.1 *Discussion* — Epitaxial growth is an example of a special case of chemical vapor deposition (CVD).

5.13 *chem-mechanical polish* — a process for the removal of surface material from the wafer that uses both chemical and mechanical actions to achieve a mirror-like surface for subsequent processing; also known as *chemo-mechanical polish* or *chemical mechanical polish*.

5.14 *chip* — region where material has been unintentionally removed from the surface or edge of the wafer.

5.15 *cleavage plane* — a crystallographically preferred fracture plane.

5.16 *concentration* — relative amount of a minority constituent of a mixture to the majority constituent (for example parts per million, parts per billion, or percent) by either volume or weight.

5.17 *conductivity (electrical), σ [$\Omega\cdot\text{cm}$]⁻¹* — a measure of the ease with which charge carriers flow in a material; the reciprocal of *resistivity*.

5.17.1 *Discussion* — In a semiconductor, the conductivity is proportional to the product of free carrier density, electron electrical charge, and carrier mobility. Most variant of all crystal properties, conductivity can range over 13 orders of magnitude. Conductivity can be locally modified by temperature, carrier injection, irradiation, or magnetic field.

5.18 *conductivity type* — a property that identifies the majority charge carrier in the semiconductor; see also *n-type*, *p-type*.

5.19 *contaminant, particulate* — see *localized light scatterer*.

5.20 *contamination, area* — matter, unintentionally added to the surface of a wafer, of extent greater than a single localized light scatterer.

5.20.1 *Discussion* — Area contamination, a type of extended light scatterer, may be foreign matter on the wafer surface resulting from chuck marks, finger or glove prints, stains, wax or solvent residues, etc.

5.21 *contamination, particulate* — a particle or particles on the surface of a wafer, see *localized light scatterer*.

5.22 *crack* — cleavage or fracture that extends to the surface of a wafer.

5.23 *crater* — surface feature with irregular closed ridges and smooth central regions.

5.24 *Crow's foot* — intersecting cracks in a pattern resembling a “crow's foot” (Y) on (111) surfaces and a cross (+) on (100) surfaces.

5.25 *crystal defect* — departure from the ideal arrangement of atoms in a crystal.

5.26 *crystal indices* — see *Miller indices*.

5.27 *crystal originated pit, COP* — a small pit or plurality of small pits introduced during crystal growth that act as an LLS when they intersect the surface of a wafer.

5.27.1 *Discussion* — Because they act in some ways similarly to particles when viewed with an SSIS, this defect was originally called a crystal originated particle. Modern SSISs can, however, generally distinguish COPs from particles. Surface cleaning or light etching frequently increases the size and number of COPs observed, when they are present.

5.28 *crystallographic notation* — a symbolism based on Miller indices used to label planes and directions in a crystal as follows:

- plane (111)
- family of planes {111}
- direction [111]
- family of directions <111>

5.29 *density, of carriers* — number of carriers per unit volume in an extrinsic semiconductor.

5.30 *density, of dopant atoms* — number of dopant atoms per unit volume in an extrinsic semiconductor.

5.30.1 *Discussion* — The density of carriers is equal to the density of dopant atoms when (1) the semiconductor is not compensated, (2) the dopant atoms are only a single type of donor or acceptor atom, and (3) the dopant atoms are 100% ionized.

5.31 *denuded zone* — a volume in a wafer, usually located just under the front surface, in which the oxygen content has been lowered so that the bulk microdefect (oxide precipitate) density is reduced.

5.32 *diameter, of a semiconductor wafer* — the linear dimension across the surface of a circular wafer that contains the wafer center and excludes flats or other peripheral fiduciary geometries.

5.32.1 *Discussion* — The measured diameter of a wafer is usually taken as the average of three or more diameter measurements. The nominal diameter is the specified diameter (e.g., 150 mm, 200 mm, or 300 mm) of the wafer around which there is an allowed tolerance (see row 2-6.1 of Table 1 of SEMI M1).

5.33 *dimple* — a shallow depression with gently sloping sides that exhibits a concave, spheroidal shape and is visible to the unaided eye under proper lighting conditions.

5.34 *dislocation* — a line imperfection in a crystal lattice that is characterized by a closure failure of Burgers' circuit.