SEMI M59-1110
TERMINOLOGY FOR SILICON TECHNOLOGY

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1 Purpose

1.1 Silicon technology underlies the integrated circuit and device industry. To promote common understanding and correct communication between suppliers and customers and others in the field, terms used in this field should be defined.

1.2 This terminology document covers definitions of terms used in relation to semiconductor silicon crystals and wafers.

2 Scope

2.1 This terminology covers general terms describing attributes of silicon wafers as specified in SEMI M1 and other SEMI Standards as outlined in SEMI M1. These attributes include electrical, structural, chemical, and dimensional characteristics of polished and other types of silicon wafers as well as surface defects and contamination. Terminology related only to a single specific test or other attribute is not generally included.

2.2 This terminology is applicable for use in connection with research, development, process control, inspection, and procurement of silicon material.

2.3 Almost all of the terms for which definitions are listed are nouns. Unless the part of speech is given for any particular term, it can be assumed that the term is a noun.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI MF1811 — Guide for Estimating the Power Spectral Density Function and Related Finish Parameters from Surface Profile Data

3.2 *ANSI Standard*[1]

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

3.3 *ISO Standard*[2]

ISO 4287-1 — Surface Roughness – Terminology – Part 1: Surface and its Parameters

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Abbreviations and Acronyms

4.1 *AAS* — atomic absorption spectroscopy, a method for analyzing for impurities.

4.2 *AFM* — atomic force microscope, an instrument for measuring microroughness.

1 American National Standards Institute, New York Office: 25 West 43rd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023; http://www.ansi.org

2 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; http://www.iso.ch

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4.3 *A/N* — alphanumeric.

4.4 *ANSI* — American National Standards Institute,[1] the American member of ISO.

4.5 *ARAMS* — automated reliability, availability, and maintainability Standard.

4.6 *As* — arsenic, an *n*-type dopant in silicon.

4.7 *ASCII* — American Standard Code for Information Interchange.

4.8 *ASTM* — ASTM International,[3] previously the American Society for Testing and Materials, an American organization that developed standards for silicon technology between 1964 and 2002; these standards, though developed primarily by American experts have been used world-wide.

4.9 *B* — boron, a *p*-type dopant in silicon.

4.10 *BMD* — bulk micro defect.

4.11 *BOX* — buried oxide layer.

4.12 *BRDF* — bi-directional reflectance distribution function.

4.13 *CCW* — counterclockwise, rotation in the direction opposite to that of the hands of a clock.

4.14 *CDF* — cumulative distribution function.

4.15 *CMOS* — complementary metal oxide semiconductor.

4.16 *COP* — crystal originated pit, a small pit or plurality of small pits introduced during crystal growth that act as an LLS.

4.17 *Cpk* — process capability index.

4.18 *CRM* — certified reference material.

4.19 *CVD* — chemical vapor deposition, a method for producing epitaxial films.

4.20 *CW* — clockwise, rotation in the direction of the hands of a clock.

4.21 *Cz* — Czochralski, a type of crystal growth.

4.22 *DI* — de-ionized, generally referred to in connection with electronic grade water.

4.23 *DIN* — Deutches Institut für Normung,[4] the German national standards organization, which has developed numerous standards for silicon during the last three decades.

4.24 *ECPK* — process capability index on a non-normal process that is corrected for non-normality.

4.25 *ERO* — edge roll-off.

4.26 *ESBIR* — near-edge silicon wafer geometry flatness metric similar to SBIR (see Appendix 1 of SEMI M1) that relates to the range of thickness values within a sector.

4.27 *ESFQD* — near-edge silicon wafer geometry flatness metric similar to SFQD (see Appendix 1 of SEMI M1) that relates to the reference plane deviation having the largest absolute value within a sector while retaining the sign.

4.28 *ESFQR* — near-edge silicon wafer geometry flatness metric similar to SFQR (see Appendix 1 of SEMI M1) that relates to the range of the reference plane deviation within a sector.

4.29 *FPD* — focal plane deviation.

4.30 *FQA* — fixed quality area of a silicon wafer.

4.31 *FT-IR* — Fourier transform infrared (spectrometer).

4.32 *FTP* — file transfer protocol.

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3 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; http://www.astm.org

4 Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D 10787 Berlin, Germany; http://www.din.de

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4.33 *FWHM* — full width of an absorption peak expressed in cm^{-1} at half its absorbance magnitude as measured from the baseline.

4.34 *FZ* — float zone, a type of crystal growth.

4.35 *GBIR* — the most common type of global flatness, see Appendix 1 of SEMI M1 for other types of global flatness.

4.36 *GEM* — generic model for communications and control of manufacturing equipment.

4.37 *GFA* — gas fusion analysis, a method for measuring total oxygen in silicon.

4.38 *GOI* — gate oxide integrity.

4.39 *GRR* — grand round robin, the international inter-laboratory experiment that established IOC-88.

4.40 *HF* — hydrofluoric acid.

4.41 *HSMS* — high speed SECS message services.

4.42 *IC* — integrated circuit.

4.43 *ICP/MS* — inductively coupled plasma mass spectroscopy, a method for analysis of impurities, not yet standardized.

4.44 *IEEE* — the Institute of Electrical and Electronic Engineers, Inc.[5]

4.45 *ID* — identification, referring to the laser mark on silicon and other semiconductor wafers.

4.46 *IOC-88* — international oxygen conversion factor-1988, the currently universally adopted conversion factor between the infrared absorption peak and the interstitial oxygen content in silicon.

4.47 *ISO* — International Organization for Standardization,[2] a body recognized by the World Trade Organization as a developer of international standards, including a few applicable to silicon technology.

4.48 *JEIDA* — Japan Electronic Industry Development Association, now JEITA.

4.49 *JEITA* — Japanese Electronic and Information Technology Industries Association,[6] successor to JEIDA upon the merging of JEIDA and the Electronic Industries Association of Japan (EIAJ), which has a committee that develops standards for silicon materials and technology.

4.50 *JIS* — Japan Industrial Standard, standards published by the Japanese Standards Association.[7]

4.51 *JPEG* — Joint Photographics Expert Group.

4.52 *LLS* — localized light scatterer.

4.53 *LOCOS* — LOCal Oxidation of Silicon.

4.54 *LPD* — light point defect, a term formerly widely used, but now superseded by the term LLS.

4.55 *L-ROA* — linear referenced ROA.

4.56 *LSE (adj.)* — light scattering equivalent.

4.57 *LSI* — large scale integration.

4.58 *LSL* — lower specification limit.

4.59 *LTFT-IR* — low temperature, Fourier transform infrared (spectrometer).

4.60 *MAE* — mixed acid etchant.

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5 IEEE Standards Association, 445 Hoes Lane, Piscataway, NJ 08855 USA. Telephone: 732.981.0060; Fax: 732.981.9667; http://www.ieee.org

6 Japan Electronics and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan; http://www.jeita.or.jp

7 Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014; http://www.jsa.or.jp

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4.61 *MCz* — magnetic Czochralski, a type of crystal growth that generally yields crystals with lower oxygen content than Cz growth.

4.62 *MOS* — metal oxide semiconductor.

4.63 *NTD* — neutron transmutation doped, a method for forming high resistivity *n*-type silicon.

4.64 *OPP* — optical precipitate profiler.

4.65 *OSF* — oxidation-induced stacking fault, a defect in silicon wafers.

4.66 *P* — phosphorus, an *n*-type dopant in silicon.

4.67 *PDF* — probability density function.

4.68 *ppba* — parts per billion atomic.

4.69 *ppbw* — parts per billion by weight.

4.70 *ppm* — parts per million.

4.71 *ppma* — parts per million atomic.

4.72 *ppmw* — parts per million by weight.

4.73 *P-ROA* — polynomial referenced ROA.

4.74 *PSD* — power spectral density.

4.75 *PSL* — polystyrene latex.

4.76 *PTFE* — polytetrafluoroethylene, an HF-resistant material for sample bottles, lids, and tongs.

4.77 *PUA* — percent usable area.

4.78 *PWP* — particles per wafer pass.

4.79 *rf* — radio frequency.

4.80 *ROA* — edge roll off amount.

4.81 *RPD* — reference plane deviation.

4.82 *RSF* — relative sensitivity factor, used in TXRF analysis of surface metals to relate the concentrations of a variety of elements to the calibration element.

4.83 *Sb* — antimony, an *n*-type dopant in silicon.

4.84 *SCFM* — standard cubic feet per minute.

4.85 *SECS* — SEMI Equipment Communications Standard.

4.86 *SECS II* — SEMI Equipment Communications Standard II.

4.87 *SFQR* — the most commonly used type of site flatness, see Appendix 1 of SEMI M1 for other types of site flatness.

4.88 *Si* — silicon.

4.89 *SIMOX* — Separation by IMplanted Oxygen.

4.90 *SIMS* — secondary ion mass spectroscopy.

4.91 *SOI* — silicon on insulator.

4.92 *SPC* — statistical process control.

4.93 *SRM* — registered trademark for a CRM produced by the National Institute for Standards and Technology.

4.94 *SSIS* — scanning surface inspection system.

4.95 *STI* — shallow trench isolation.

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4.96 *TDDB* — time dependent dielectric breakdown.

4.97 *TIR* — total indicator reading (also known as total indicator runout).

4.98 *TTV* — total thickness variation.

4.99 *TXRF* — total reflection X-ray reflectance spectroscopy, a surface metal analysis technique.

4.100 *TZDB* — time zero dielectric breakdown.

4.101 *USL* — upper specification limit.

4.102 *VPD* — vapor phase decomposition.

4.103 *XLS* — extended light scatterer.

4.104 *XML* — eXtensible Markup Language.

4.105 *ZDD* — measure of near-edge curvature of a silicon wafer equal to the radial double derivative of the coordinate z perpendicular to the median plane of the wafer.

5 Definitions

5.1 *1/e lifetime (τ_e)* — the time duration from the laser pulse injection to the instant that the excess carrier density decreases to $1/e$.

5.2 *acceptor* — an impurity in a semiconductor that accepts electrons excited from the valence band, leading to hole conduction.

5.3 *accumulation condition* — the region of the capacitance-voltage (C-V) curve for which a 5 V increment toward a more negative voltage for *p*-type material, or toward a more positive voltage for *n*-type material, results in a change of less than 1% in the maximum capacitance, C_{max}.

5.4 *air reference spectrum* — an absorption spectrum obtained with only nitrogen, dry air, or a vacuum in the beam of the spectrometer. In FT-IR spectrometers, also called *background spectrum*.

5.5 *alignment precision, in buried epitaxial wafer technology* — pattern displacement in first mask photolithography process.

5.6 *alpha error* — error that occurs when a conforming item is incorrectly reported as non-conforming; also called *Type I error.*

5.7 *alpha probability* — probability of an alpha error, also called *alpha error rate.*

5.8 *anisotropic* — exhibiting different physical properties in differing crystallographic directions.

5.9 *anisotropic etch* — a selective etch that exhibits an accelerated etch rate along specific crystallographic directions used to determine crystal orientation, to fabricate micromechanical structures, and to facilitate dielectric component isolation.

5.10 *annealed wafer* — wafer that has a defect (COP) free zone near the surface resulting from high temperature annealing under a neutral or reducing atmosphere.

5.11 *annealing* — a high temperature process that alters the characteristics of the wafer.

5.12 *apex* — the blunt, but not necessarily linear, segment of an edge profile, oriented approximately perpendicular to the reference line and located between the front and back shoulders.

5.13 *apex angle, of an edge profile* — the angle between the z-axis and the front or back apex; the sign of the apex angle is positive if the q-coordinate increases with increasing magnitude of $|z|$.

5.14 *apex length, of an edge profile* — the distance along the z-axis between the front and back shoulders of the edge profile, usually divided into two distances from the reference line to the front and back shoulders.

5.15 *autodoping, of an epitaxial layer* — incorporation of dopant originating from the back or front surfaces and edges of the substrate, other substrates in the reactor, the susceptor, or other parts of the deposition assembly substrate into the epitaxial layer. Also called *self-doping*.

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5.15.1 *average roughness (R_a)* — mean value of surface profile height deviations $Z(x)$ from the mean line taken within the evaluation length.

5.16 *back surface* — the exposed surface opposite to that upon which active semiconductor devices have been or will be fabricated.

5.17 *background spectrum* — in FT-IR instruments, the single-beam absorption spectrum obtained without a specimen in the infrared light path that is usually obtained with only nitrogen, dry air, or a vacuum in the beam.

5.18 *backseal* — a film of silicon dioxide or other insulator placed over the back surface of a silicon wafer to inhibit outdiffusion of the majority dopant impurity.

5.19 *backside* — not preferred, use *back surface*.

5.20 *base silicon substrate* — the wafer used as a support for the multilayer structure of oxide and silicon that comprises an SOI wafer. In the case of SIMOX technology, it is the starting wafer into which the oxygen is implanted. Also known as *handle wafer*.

5.21 *baseline* — straight line interpolation between points on either side of the peak of an absorbance spectrum due to an impurity such as carbon, nitrogen, or oxygen in silicon, drawn to represent the spectrum that would have been obtained in the absence of the impurity.

5.22 *baseline absorbance* — value of the baseline at the wavenumber corresponding to the impurity absorbance peak that is used for evaluating the peak height.

5.23 *beta error* — error that occurs when a non-conforming item is incorrectly reported as conforming; also called *Type II error.*

5.24 *beta probability* — the probability of a beta error, also called *beta error rate.*

5.25 *bevel, of an edge profile* — the segment of the edge profile located between the surface line and the shoulder.

5.26 *bevel angle, of an edge profile* — the angle between the median plane and the front or back bevel of the edge profile.

5.27 *bevel angle (α), of a bevel-polished wafer section* — the smaller of the angles between the wafer surface and the section plane on the bevel polished specimen.

5.28 *bias* — difference between the population mean of the test results from a measurement process and the true (accepted reference) value of the property being measured.

5.29 *bias temperature stress, (BTS)* — voltage applied to the top surface of a dielectric layer on a silicon wafer whose temperature is maintained at a defined level for a specified time.

5.30 *bi-directional reflectance distribution function, BRDF* — a description of the distribution of light scattered by a surface, it is the differential radiance normalized by the differential irradiance, and is approximated by the scattered power per unit projected solid angle divided by the incident power.

5.31 *bonded interface* — the plane where the bonding between two wafers takes place, also called *bonding interface*.

5.32 *bonded SOI wafer* — an SOI wafer made by bonding two silicon wafers with an insulating layer that is typically thermally grown silicon dioxide between them.

5.33 *bonding interface* — see *bonded interface*.

5.34 *bow* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer.

5.35 *BOX pin-hole* — electrically conductive path through the BOX.

5.36 *bulk recombination lifetime* (τ_b) — the lifetime in the case that surface recombination is negligible and depends only on defects and impurity densities in the crystal bulk.

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5.37 *buried layer, in buried epitaxial wafer technology* — a diffused region in a substrate that is, or is intended to be, covered with an epitaxial layer.

5.38 *buried oxide layer* — the silicon dioxide layer between the SOI layer and the base silicon substrate.

5.39 *calibration* — set of operations that establish the relationship between values of quantities indicated by a measurement system and the corresponding values assigned to reference materials to eliminate or reduce bias in the measurement system relative to the reference base.

5.40 *capability based sampling* — any method that uses the process capability as a factor in determining the required sampling.

5.41 *capture rate (CR)* — probability that an SSIS detects an LLS of latex sphere equivalent (LSE) signal value at some specified SSIS operational setting.

5.42 *carrier* — (1) *charge carrier*; (2) *wafer carrier*. When the context is not sufficient to clearly indicate which meaning is to be used, it is appropriate to utilize the full term.

5.43 *carrier density* — number of majority charge carriers per unit volume in an extrinsic semiconductor. The symbol n is used for electron density (although it sometimes is used more generally as carrier density), and the symbol p is used for hole density. These quantities are usually given in number/cm^3 although the SI unit is number/m^3.

5.44 *center-referenced* (*adj.*) — property of a measurement, calculation, or coordinate system with the position established using the wafer center as the origin, such as in the wafer coordinate systems of SEMI M20.

5.45 *certified deposition*, *in surface scanning of silicon wafers* — a reference sphere deposition on an unpatterned wafer with the same surface films and finish as the wafers to be examined by a calibrated SSIS with specific property values certified by a technically valid procedure, accompanied by or traceable to a certificate that is issued by a certifying body.

5.46 *certified reference material (CRM)* — reference material one or more of whose property values are certified by a technically valid procedure, accompanied by or traceable to a certificate or other documentation issued by a certifying body and for which each certified value is accompanied by an uncertainty at a stated level of confidence.

5.47 *certifying body* — organization that is recognized to have the ability to carry out a technically valid procedure or procedures to establish property values of a reference material traceable to an accurate realization of the unit in which the property values are expressed.

5.48 *charge carrier* — an entity capable of carrying electric charge through a solid, for example, valence holes and conduction electrons in semiconductors.

5.49 *chemical vapor deposition* (*CVD*)*, in semiconductor technology* — a process in which a controlled chemical reaction produces a thin surface film, such as growth of an epitaxial layer.

5.50 *chem-mechanical polish* — a process for the removal of surface material from the wafer that uses both chemical and mechanical actions to achieve a mirror-like surface for subsequent processing; also known as *chemo-mechanical polish* or *chemical mechanical polish*.

5.51 *chip* — region where material has been unintentionally removed from the surface or edge of the wafer.

5.52 *cleavage plane* — a crystallographically preferred fracture plane.

5.53 *compatibility* — capability of a measurement system to emulate the measurement process of other measurement systems.

5.54 *compensation* — reduction in number of free carriers resulting from the presence of impurities other than the majority dopant density impurity.

5.55 *concentration* — relative amount of a minority constituent of a mixture to the majority constituent (e.g., parts per million, parts per billion, or percent) by either volume or weight.

5.56 *conductivity* (*electrical*), σ [$(\Omega\cdot\text{cm})^{-1}$] — a measure of the ease with which charge carriers flow in a material; the reciprocal of *resistivity.* In a semiconductor, the conductivity is proportional to the product of free carrier density, electron electrical charge, and carrier mobility. Most variant of all crystal properties, conductivity can range over 13

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