SEMI M60-0306
TEST METHOD FOR TIME DEPENDENT DIELECTRIC BREAKDOWN CHARACTERISTICS OF SiO_2 FILMS FOR Si WAFER EVALUATION

This standard was technically approved by the global Silicon Wafer Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on November 29,2005. It was available at www.semi.org in February 2006 and on CD-ROM in March 2006. Originally published January 2005; previously published March 2005.

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1 Purpose

1.1 The technique outlined in this test method is for the purpose of standardizing silicon wafer characterization by GOI (Gate Oxide Integrity). For more detailed discussion of the general characterizing methods for this test, the reader is referred to §3. TZDB technique as SEMI M51 is advantageous to estimate failure rate by intrinsic breakdown as the C mode and an accidental breakdown as the B mode. However, this test method has a higher sensitivity for detecting the accidental breakdown mode than TZDB.

2 Scope

2.1 This test method is for the purpose of the characterization method of silicon wafer by GOI. This characterization method is outlined below

2.1.1 *MOS (Metal Oxide Semiconductor) — capacitor fabrication* — A gate oxide film is thermally grown on a silicon wafer surface. Then, poly-Si electrodes are formed on the gate oxide film. Other metals, other than poly-silicon electrode materials, can be used, however, it shall be desirable to use an electrode that has been confirmed to have sufficiently good characteristics for application as a gate electrode as described below.

2.1.2 *Electrical Characterization Evaluation* — The TDDB (Time Dependent Dielectric Breakdown) characteristics of the MOS capacitors are measured. The presence of COPs (Crystal Originated Particles) at the surface of the polished Si substrates influences the TDDB characteristics of the gate oxide. That is, the silicon wafer is evaluated in terms of the TDDB characteristics of the gate oxide. The test method outlined in this test method is for the purpose of standardizing the procedure of MOS fabrication, measurement, analyses, and the report of the GOI data to interested parties. This test method is based on the results of round robin among the silicon wafer manufacturers. In general, GOI strongly depends on crystal defects, contaminations and particles on/near wafer surface. GOI also depends on the fabrication environment. The cleanliness of the process environment in which the MOS capacitors are fabricated shall be evaluated to be acceptable (see ¶5.3).

2.2 The target of this test method is to characterize silicon wafers, that is, evaluate COPs near the silicon wafer surface. The proper gate oxide thickness of the MOS samples is 20–25 nm. A discussion on gate oxide thickness is given in a later section. Oxygen precipitates are also one of the gate oxide defect origins, however, this is beyond the scope of this test method because the as-received wafers contain only a small amount of oxygen precipitates. Near-surface quality can be evaluated in this test. In this case, it is assumed that an oxide film thickness of approximately 10 nm is used. It is more difficult to categorize the accidental and intrinsic breakdowns in TZDB, as the gate oxide thickness becomes thinner. Therefore mode classification in TDDB is more effective.

2.3 For detailed discussion on sample structures used in this test method, the reader shall refer to EIA/JEDEC Standard 35-1. In general, the most likely sample structures are a simple planar MOS (Metal Oxide Semiconductor) capacitor structure, various isolation structures (for example, LOCOS (LOCal Oxidation of Silicon), STI (Shallow Trench Isolation)), and FET (Field-Effect Transistor) structures. For the purpose of silicon wafer characterization, the simple planar MOS capacitor structure is the most desirable. In the case of the various isolation and FET structures, the silicon wafer receives thermal treatments several times in the complicated sample fabrication process. Therefore, in this case it is questionable whether the characteristics of the starting Si wafer are reflected in this test measurement results.

2.4 In this evaluation method, a constant current stress is applied to the gate oxide and time to breakdown is measured. The amount of charge injected until dielectric breakdown (Q_{bd}) is also calculated. (Constant-current TDDB: detail of measurement condition is described in a later section). The dielectric breakdown by the COPs and other defects can be evaluated from the accumulated failure distribution of Q_{bd}. In addition, a constant-voltage TDDB method can be used as an evaluation of gate oxide lifetime. In this test method, the constant-current TDDB

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method is chosen, because the constant current TDDB method has less influence on parasitic resistance in a measurement circuit than the constant-voltage TDDB method.

2.5 This test method gives instructions for the procedure for characterizing mirror-polished, p-type CZ silicon wafers. Gate electrodes were negatively biased so that the silicon surface is in accumulation. Stress current shall be sufficient for the gate oxide to be broken down within a finite measurement time. In addition, it is desirable to have an applied current density J within 0.001 and 0.1A/cm^2.

2.6 The stress gate current has to be reversed for the n-type silicon wafer.

2.7 The poly-silicon film is used as gate electrode of measured MOS capacitors. The poly-silicon film can make standard test results applicable to the testing of wafers used to fabricate integrated circuits rather than other metal electrodes because poly-silicon electrodes are commonly used in actual devices. However, a gate electrode other than poly-silicon gate electrode shall be studied for applications in advanced ultralarge-scale integrated circuits. In this case, the new electrode material shall have the same detection sensitivity to silicon wafer defects as poly-silicon electrode.

NOTICE: This test method does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this test method to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

NOTE 1: When there is no special direction, all the quoted documents are the newest editions.

NOTE 2: When a material other than poly-silicon is used for electrodes, refer to the standard suitable for individual process.

3.1 *SEMI Standards*

SEMI C3.6 — Standard for Phosphine (PH_3) in Cylinders, 99.98% Quality

SEMI C3.40 — Standard for Carbon Tetrafluoride (CF_4, VLSI GRADE)

SEMI C3.54 — Gas Purity Guideline for Silane (SiH_4)

SEMI C21 — Specifications and Guideline for Ammonium Hydroxide

SEMI C27 — Specifications and Guidelines for Hydrochloric Acid

SEMI C28 — Specifications and Guidelines for Hydrochloric Acid

SEMI C30 — Specifications and Guidelines for Hydrogen Peroxide

SEMI C35 — Specifications and Guideline for Nitric Acid

SEMI C38 — Guideline for Phosphorus Oxychloride

SEMI C41 — Specifications and Guidelines for 2-Propanol

SEMI C44 — Specifications and Guidelines for Sulfuric Acid

SEMI C54 — Specifications and Guidelines for Oxygen

SEMI C59 — Specifications and Guidelines for Nitrogen

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M51 — Test Method For Characterizing Silicon Wafers by Gate Oxide Integrity.

SEMI M59 — Terminology for Silicon Technology

SEMI MF1771 — Standard Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique

3.2 *ASTM Standards*[1]

ASTM D5127 — Standard Guide for Ultra Pure Water Used in the Electronics and Semiconductor for Industry.

3.3 *EIA/JEDEC Standards*[2, 3]

EIA/JEDEC 35 — Procedure for the Wafer-Level Testing of Thin Dielectrics

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

2 Electronic Industries Alliance, EIA Engineering Department, Standards Sales Office, 2001 Eye Street, NW, Washington, D.C. 20006, USA. Website: www.eia.org

3 Joint Electron Device Engineering Council, 2500 Wilson Blvd., Arlington, VA 22201, website: www.jedec.org

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EIA/JEDEC 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-2 — Test Criteria for the Wafer-Level Testing of Thin Dielectric

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Abbreviations & Acronyms*

4.1.1 *COP* — Crystal Originated Particles

4.1.2 *GOI* — Gate Oxide Integrity

4.1.3 *LOCOS* — Local Oxidation of Silicon

4.1.4 *MOS* — Metal Oxide Semiconductor

4.1.5 *STI* — Shallow Trench Isolation

4.1.6 *TZDB* — Time Zero Dielectric Breakdown

4.2 *Definitions*

4.2.1 Many terms relating to silicon technology are defined in SEMI M59.

4.2.2 Definitions for some additional terms are given in SEMI M1 and SEMI MF1771.

4.2.3 Other terms are defined as follows:

4.2.3.1 *Crystal Originated Particles*[4] *(COP)* — this is the one of grown-in defects in the CZ Si wafers with an octahedral structure. This was found as particles appeared on the silicon surface by repetition SC-1[5] of RCA cleaning.

4.2.3.1.1 *Discussion* — It has been thought that the COP is one of the main origins of the GOI. The gate oxide formed on the Si surface at which the COP appears easily breaks down at the corner of the octahedral shape like at a Si trench corner[6,7,8]. This corner of octahedral structures is thinning the oxide films. The oxide electric field enhances at that place. The breakdown electric field is decreased.

4.2.3.2 *Failure Modes* — the TDDB Weibull plot[9, 10] is classified to three modes. A typical plot is shown in Figure 1.

Accidental failure — A-A mode
A-B mode
Wearout breakdown — W mode

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4 J. Ryuta, E. Morita, T. Tanaka and Y. Shimanuki, "Crystal – Originated Singularities on Si Wafer Surface after SC1 Cleaning", *Jpn. J. Appl. Phys.* 29(1990) L947.

5 W. Kern and D. Puotinen, "Clean Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology", *RCA Rev.*, 31, 187(1970).

6 T. Mera, J. Jablonski, K. Nagai, and M. Watanabe, "Grown-in defects in silicon crystals responsible for gate oxide integrity deterioration", *Ohyo-Buturi*, 66(7), 728 (1997).

7 K.Yamabe and K.Imai,"Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation", IEEE Trans. Electron Devices, ED–34, 1681(1987).

8 K.Yamabe, Y.Shimada, M.Piao, T.Yamazaki, T.Otsuki, R.Takeda, Y.Ohta, S.Jimbo, and M.Watanabe, "Effect of SiO2 Thickness on Dielectric Breakdown Defect Density Due to Surface Crystal–Originated Particles", J.Electrochem.Soc., 150, F42(2003).

9 D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", Proc. *Int. Reliability Physics Symposium*, 1979, p.1.

10 E. S. Anolick and G. R. Nelson, "Low Field Time Dependent Dielectric Integrity", Proc. *Int. Reliability Physics Symposium*, 1978, p.8.

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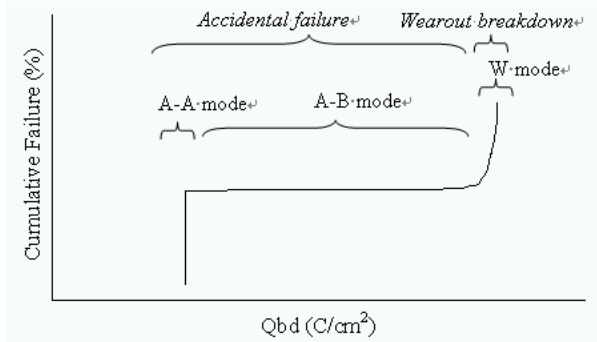

Figure 1

Classification in Weibull Plot of TDDB Result.

4.2.3.2.1 Discussion on failure modes:

- *A-A Mode*: Initial breakdown failure
  - This failure is caused by defects generated during gate oxide formation process such as pinholes and also by crystal defects such as COPs. This failure corresponds to the A mode and partly B mode failures of TZDB.
- *A-B Mode*: Intermediate breakdown failure
  - This failure is caused by extrinsic defects which are not serious enough to cause the A-A mode. This failure corresponds to the B mode and partly C mode failure of TZDB.
- *W Mode*: Wearout breakdown
  - This breakdown is also called intrinsic breakdown or fatigue breakdown, and relates to the intrinsic lifetime of oxide films. The measurement of this breakdown shall be performed carefully because the result depends on measurement conditions.
  - Response rapidity of the measurement system has a great influence on A-A mode detection. The total number of A-A and A-B mode failures is related to the crystal quality of the mirror-polished CZ Si wafers.

4.2.3.3 *Categorization of Breakdown Modes* — boundaries of A-A/A-B modes and A-B/W modes shall be defined in advance.

4.2.3.3.1 *A-A/A-B Mode Boundary*

- The detectable minimum Q_{bd} values depend on the stress current and response speed of the measurement systems. As stress current density increases, the charge density of the A-A/A-B mode boundary may also increases. This effect shall be considered when defining the A-A/A-B mode boundary. Based on these round robin results, the charge density range from 0.0001C/cm^2 to 0.01 C/cm^2 is recommended as the A-A/A-B mode boundary.

4.2.3.3.2 *A-B/W Mode Boundary*

- The A-B/W mode boundary is defined in terms of Weibull plots as shown in Figure RI-3. Ideally, it shall be determined by the intercept point of two approximation lines in the A-B and W mode ranges. If the boundary charge density is too low ($Q < 1$ C/cm^2), one part of the A-B mode breakdown can be counted as the W mode. Otherwise, if the boundary charge density is too high ($Q > 4$ C/cm^2), one part of the W mode breakdown can be counted as the A-B mode.
- In both cases, we have errors in the classification of the failure mode categories, even if the measurement is accurately carried out and appropriate Weibull plots are obtained. So, the results of this round robin indicate that the charge density of 2 C/cm^2 is recommended as the A-B/W mode boundary. To measure the failure rates at the boundary charge density of the A-B/W modes, all samples are not necessarily broken down. If the determination procedure of the boundary charge density is clear, the application of a predetermined charge density will give us the approximate failure rate by the A-B mode breakdown. It is necessary to determine the classification of failure modes in advance. This is because reliabilities depend on the devices fabricated on the Si wafer (electrode material, gate oxide thickness, operating voltage, etc.). Refer to an example of mode classification described in Figure RI-2.

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4.2.3.4 *Time Zero Dielectric Breakdown (TZDB)* — one of the dielectric breakdown characteristic of the gate oxide.

4.2.3.4.1 *Discussion* — To measure TZDB, oxide leakage current is monitored with an electric field applied to the MOS capacitor stepwise from 0 to 15MV/cm (for example in the case of a 25 nm-thick oxide, actual applied voltage would be from 0 to 37.5V). The electrode is negatively biased so that the Si surface is in accumulation and the electric field is applied effectively. Applied electric field (or voltage) is measured when the oxide leakage current reaches a predetermined value (judgment current), in other words when the gate oxide breaks down. The influence of COPs on gate oxide breakdown can be estimated from the distribution of breakdown electric field.

5 Summary of Method

5.1 *Overview* — This test method consists of two parts. The first one is the fabrication of a number of similar MOS capacitors on silicon wafers, and the second one is the measurement of the electric charge injected just before the dielectric breakdown of the MOS capacitors. To measure the injected electric charge, the voltage applied to a MOS capacitor is controlled so that the current is kept constant. The voltage is monitored throughout the test, and the time from the beginning to a sudden voltage drop which results from the dielectric breakdown of the silicon dioxide film is measured. The injected electric charge is the product of the measured time and the gate current density.

5.2 *MOS Capacitor Fabrication Process* — Many MOS capacitors are formed on the test wafer. The MOS fabrication process consists of wafer cleaning, thermal oxidation, poly-Si deposition, phosphorous doping, activation heat treatment, photolithography and etching, in the case of using poly-Si electrodes. The details of the MOS capacitor fabrication process are shown in SEMI M51. When materials other than poly-silicon are used for electrodes, the process shall be adjusted to the material used. Although thermally grown 20–25 nm-thick gate oxide films are recommended in SEMI M51, oxide films as thin as 10 nm can be used depending on the situation. However, measurement shall be performed carefully for oxide films thinner than 3 nm, because breakdown judgment becomes difficult under the influence of direct tunneling current. See SEMI C3.40, SEMI C3.6, SEMI C3.54, SEMI C21, SEMI C27, SEMI C28, SEMI C30, SEMI C35, SEMI C38, SEMI C41, SEMI C44, SEMI C54, SEMI C59.

5.3 *Fabrication Environment* — It is necessary to fabricate MOS capacitors in a clean room environment of 1000 or better class in total quality. That is, it needs to be confirmed that the A mode failure rate is 10% or less by TZDB evaluation. The A mode failure depends not only on the particle of work environment atmosphere but also on the ultrapure water, fixtures, process apparatus, clean clothes, operation rules etc. Heavily contamination such as alkaline or heavy metal has an important negative effect on the GOI of the oxide.

5.4 *Measurement of Electric Characteristic of MOS Capacitors*

5.4.1 The dielectric breakdown defect density of the silicon oxide film is evaluated by constant current TDDB measurement of the MOS capacitors. The evaluation consists of the measurement of charge injected before the dielectric breakdown of the MOS capacitors. To measure the injected charge, voltage applied to a MOS capacitor is controlled so that the current is kept constant. The applied voltage is monitored throughout the test, and the time to sudden voltage drop which results from dielectric breakdown of the silicon dioxide film is measured. The amount of the injected charge is the product of the measured time and gate current density. The defect density of the oxide film is evaluated from the Weibull plot (cumulative failure rate) of the dielectric breakdown data of approximately 100 MOS capacitors.

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5.4.2 *Stress Current Density* — For reliable measurement, a voltage/current source with a stable output wave shape shall be used. It is necessary to stabilize the output as much as possible. In the constant current TDDB measurement, a constant current is continuously applied, and voltage is monitored. The dielectric breakdown is judged by a sudden drop in the voltage monitored. If the applied stress current density is too low, the time to breakdown will be too long to be realistic. Contrarily, too a high current density is also unsuitable because the voltage drop in the oxide breakdown instant becomes small. Considering these factors, the recommended stress current density range is from 0.001 to 0.1A/cm^2.

5.5 *Measurement Temperature* — Besides current density, the measurement temperature is also an important parameter which determines measurement time. It is appropriate to measure in the temperature range of room temperature to 150ºC, taking into consideration the temperature tolerance of the measurement equipment. In addition, there are cases that since silicon wafer, stage chuck, probe, and so on, expand at a high temperature, the probe deviates from the predetermined position, thus consideration is required when selecting probing machines.

5.6 *Breakdown Judgment* — To measure the dielectric breakdown lifetime of an oxide film, the voltage applied to a MOS capacitor is controlled so that a current is kept constant. The applied voltage is monitored throughout the test. The dielectric breakdown of the oxide is judged by sudden voltage drop. In practice, at the dielectric breakdown the applied voltage becomes lower than the criterion voltage defined before. The dielectric breakdown lifetime is the stress application time till breakdown. If the criterion voltage is too low, it can easily affected by noise. In contrast, the chance of missing breakdown events is increased if the criterion voltage is too high. The changes in two continuous measured gate voltages can be used to judge the oxide breakdown. The instant at which the voltage change became larger than the criterion value is defined as dielectric breakdown. The same caution mentioned above is also required in this case. In this round robin, the current density is from 0.001 to 0.1A/cm^2, the sheet resistance of the poly-silicon electrode is approximately 50 ohm/sq, gate electrode area is from 1mm^2 to 10mm^2, gate oxide thickness is 25nm and measurement temperature is from room temperature to 150ºC. In this case dielectric breakdown is determined from the changes in two continuous measured gate voltages. For example, the change in gate voltage is larger than $X_{criterion}$(%) of the former gate voltage value. $X_{criterion}$ is higher than 10%. Alternatively, dielectric breakdown is determined with the measured electric field, E_{ox}. It is considered that dielectric breakdown does not happen until E_{ox} becomes $E_{criterion}$ or lower. $E_{criterion}$ is higher than 4MV/cm. Stable measurement results are obtained in both cases. Of course, these criterion electric fields depend on gate oxide thickness, sheet resistance and area of gate electrode, stress current, stress temperature, and so on. To detect the dielectric breakdown with the change in gate voltage as shown in Figure 2, it is desirable to determine the criterion under each condition in advance.

5.7 *Estimation of Accidental Failure Rate* — As mentioned before, the total number of A-A and A-B mode failures is related to the crystal quality of the mirror polished CZ Si wafers. It takes a long time to measure the wearout lifetime of all the MOS capacitors. If a requirement is only measurement of the accidental failure rates of the MOS capacitors on silicon wafer surface, TDDB measurement can be finished without detecting the wearout lifetimes. That is, maximum stress time, T_{max}, is determined to be Q_{bd} in the A-B mode range in advance. The cumulative failure rate at T_{max} is the total failure rate of the A-A and A-B modes. If the rough shapes of the Weibull plots of the TDDB measurement can be predicted in advance, T_{max} shall be determined as to be the maximum Q_{bd} in the relatively flat range of the A-B mode. This reason is that variation of T_{max} has little influence on the evaluation of total accidental failure rates. This method has an advantage of that the failure rate of the A-A and A-B modes is evaluated very quickly.

5.8 *Constant-Voltage TDDB* — The constant-voltage TDDB method is also used for a lifetime test. Measurement conditions shall be optimized for each purpose. For TDDB, an average electric field of approximately 10MV/cm is required. Therefore, the effective electric field applied to an oxide film is influenced by a series resistance. Thus, the constant current TDDB is more suitable.

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