SEMI M60-1113
TEST METHOD FOR TIME DEPENDENT DIELECTRIC BREAKDOWN CHARACTERISTICS OF AMORPHOUS SIO_2 FILMS FOR SILICON WAFER EVALUATION

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on August 22, 2013. Available at www.semiviews.org and www.semi.org in November 2013. Originally published January 2005; previously published March 2007.

SUPERSEDED

1 Purpose

1.1 This Test Method details the time dependent dielectric breakdown (TDDB) gate oxide integrity (GOI) approach to silicon wafer characterization. The time zero dielectric breakdown (TZDB) GOI test method of SEMI M51 is advantageous compared to TDDB to quickly estimate failure rate by intrinsic breakdown (C mode) and accidental breakdown (B mode). However, this TDDB test method has a higher sensitivity for detecting the accidental breakdown (B mode) than TZDB.

2 Scope

2.1 This Test Method provides detailed procedures for characterizing silicon wafers GOI using the TDDB method. This Test Method describes standard procedures for metal oxide semiconductor (MOS) capacitor fabrication, electrical measurement, analysis, and reporting.

2.2 Thermally grown gate oxide (amorphous SiO_2) with film thicknesses of 20 to 25 nm followed by polysilicon electrode film deposition is used to make MOS capacitors on a test wafer.

2.3 The target of this Test Method is to characterize silicon wafers: that is, evaluate the electrical performance impact of defects at or near the silicon wafer surface.

2.4 Both constant-current and constant-voltage TDDB methods can be used as an evaluation of gate oxide lifetime. However, in this Test Method, the constant-current TDDB method is chosen, because the constant current TDDB method is less influenced by parasitic resistance in the measurement circuit than is the constant-voltage TDDB method.

2.5 This Standard is based on round robin results among silicon wafer manufacturers.

2.6 In general, TDDB results are strongly influenced by the presence of surface defects such as COPs. Other wafer surface defects may also contribute to TDDB results.

2.6.1 Determining the root cause of TDDB results is beyond the scope of this Test Method.

2.6.2 Determining the MOS fabrication impact to TDDB results is beyond the scope of this Test Method.

NOTE 1: Polysilicon electrodes are a required part of this Standard.

NOTE 2: For a detailed discussion of sample structures for this Test Method, the reader is referred to JESD 35-1. In general, the three most likely MOS sample structures are simple planar MOS capacitors, MOS capacitors with various isolation structures and field effect transistors. For the purpose of silicon wafer characterization, the simple planar MOS capacitor structure is preferable.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Results from this TDDB GOI test method strongly depend on the wafer-surface and near-surface crystal defects, particles, contamination and cleanliness. Therefore cleanliness of the GOI processes environment during MOS fabrication may impact wafer test results negatively, introducing TDDB failures that are GOI process related rather than wafer manufacturing process related.

Documents Document Sharing Hub
Full document details: SEMI M60-1113

3.2 Results may not be valid unless the equipment used to measure critical parameters of the test structures and test results remains calibrated.

4 Referenced Standards and Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI M51 — Test Method for Time Zero Dielectric Breakdown Characteristics of Amorphous SiO_2 Films for Silicon Wafer Evaluation

SEMI MF1771 — Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique

4.2 *ASTM Standard*[1]

ASTM D5127 — Standard Guide for Ultra Pure Water Used in the Electronics and Semiconductor Industries

4.3 *ISO Standard*[2]

ISO 14644–1 — Cleanrooms and Associated Controlled Environments – Part 1: Classification of Air Cleanliness

4.4 *JEDEC Standards*[3]

JESD 35-A — Procedure for the Wafer-Level Testing of Thin Dielectrics

JESD 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

JESD 35-2 — Test Criteria for the Wafer-Level Testing of Thin Dielectrics

JEDEC/FSA Joint Publication JP001.016 — Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Acronyms, terms, and symbols related to silicon technology, including those used in these practices, are listed and defined in SEMI M1 and SEMI M59.

6 Comprehensive Explanation of Terms

6.1 *COP* — It has been thought that COPs4 are one of the main origins of GOI degradation. The gate oxide formed on the silicon surface at which the COPs appear breaks down easily at the corner of an octahedral shape like a silicon trench as the oxide thickness becomes thinner there.[5, 6, 7] The oxide electric field is enhanced at that place and the breakdown voltage becomes less.

SUPERSEDED

[1] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: 610.832.9585, Fax: 610.832.9555, http://www.astm.org

[2] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, http://www.iso.ch

[3] Joint Electron Device Engineering Council, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201, USA; Telephone: 703.907.7560, Fax: 703.907.7583, http://www.jedec.org

[4] Ryuta J., Morita E., Tanaka T. and Shimanuki Y., "Crystal – Originated Singularities on Si Wafer Surface after SC1 Cleaning." *Jpn. J. Appl. Phys*. 29(1990) L1947.

[5] Mera T., Jablonski J., Nagai K., and Watanabe M., "Grown-in defects in silicon crystals responsible for gate oxide integrity deterioration." *Ohyo-Buturi*, 66(7): (1997) p. 728.

[6] Yamabe K. and Imai K., "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation." *IEEE Trans. Electron Devices*, ED-34 (1987) p. 1681.

[7] Yamabe, K., Shimada, Y., Piao, M., Yamazaki, T., Otsuki, T., Takeda, T., Ohta, Y., Jimbo, S., and Watanabe, M. "Effect of SiO2 Thickness on Dielectric Breakdown Defect Density Due to Surface Crystal-Originated Particles." Journal of The Electrochemical Society, 150, F42-F46 (2003).

Documents
Document Sharing Hub
Full document details: SEMI M60-1113

6.2 *Failure Modes* — the TDDB Weibull plot[8, 9] is classified to three modes. A typical plot is shown in Figure 1.

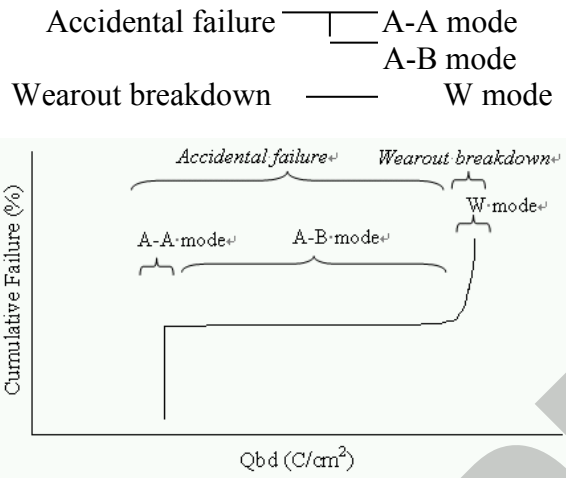

Figure 1
Classification in Weibull Plot of TDDB Result

6.2.1 Discussion on failure modes:

- *A-A Mode*: Initial breakdown failure
  - This failure is caused by defects generated during gate oxide formation process such as pinholes and also by crystal defects such as COPs. This failure corresponds to the A mode and partly B mode failures of TZDB.
- *A-B Mode*: Intermediate breakdown failure
  - This failure is caused by extrinsic defects which are not serious enough to cause the A-A mode. This failure corresponds to the B mode and partly C mode failure of TZDB.
- *W Mode*: Wearout breakdown
  - This breakdown is also called intrinsic breakdown or fatigue breakdown, and relates to the intrinsic lifetime of oxide films. The measurement of this breakdown shall be performed carefully because the result depends on measurement conditions.
  - Response rapidity of the measurement system has a great influence on A-A mode detection. The total number of A-A and A-B mode failures is related to the crystal quality of the mirror-polished CZ Si wafers.

6.2.1.1 *Categorization of Breakdown Modes* — boundaries of A-A/A-B modes and A-B/W modes shall be defined in advance.

6.2.1.1.1 *A-A/A-B Mode Boundary*

- The detectable minimum Q_{bd} values depend on the stress current and response speed of the measurement systems. As stress current density increases, the charge density of the A-A/A-B mode boundary may also increases. This effect shall be considered when defining the A-A/A-B mode boundary. Based on these round robin results, the charge density range from 0.0001C/cm^2 to 0.01 C/cm^2 is recommended as the A-A/A-B mode boundary.

[8] D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown." Proc. *Int. Reliability Physics Symposium* (1979): p.1.

[9] E. S. Anolick and G. R. Nelson, "Low Field Time Dependent Dielectric Integrity." Proc. *Int. Reliability Physics Symposium* (1978): p.8.

SUPERSEDED

Documents Document Sharing Hub
Full document details: SEMI M60-1113

6.2.1.1.2 *A-B/W Mode Boundary*

- The A-B/W mode boundary is defined in terms of Weibull plots as shown in Figure RI-3. Ideally, it shall be determined by the intercept point of two approximation lines in the A-B and W mode ranges. If the boundary charge density is too low ($Q < 1$ C/cm^2), one part of the A-B mode breakdown can be counted as the W mode. Otherwise, if the boundary charge density is too high ($Q > 4$ C/cm^2), one part of the W mode breakdown can be counted as the A-B mode.

- In both cases, we have errors in the classification of the failure mode categories, even if the measurement is accurately carried out and appropriate Weibull plots are obtained. So, the results of this round robin indicate that the charge density of 2 C/cm^2 is recommended as the A-B/W mode boundary. To measure the failure rates at the boundary charge density of the A-B/W modes, all samples are not necessarily broken down. If the determination procedure of the boundary charge density is clear, the application of a predetermined charge density will give us the approximate failure rate by the A-B mode breakdown. It is necessary to determine the classification of failure modes in advance. This is because reliabilities depend on the devices fabricated on the Si wafer (electrode material, gate oxide thickness, operating voltage, etc.). Refer to an example of mode classification described in Figure RI-2.

6.3 *Time Zero Dielectric Breakdown (TZDB)* — One of the dielectric breakdown characteristic of the gate oxide.

6.3.1 *Discussion* — To measure TZDB, oxide leakage current is monitored with an electric field applied to the MOS capacitor stepwise from 0 to 15 MV/cm (e.g., in the case of a 25 nm-thick oxide, actual applied voltage would be from 0 to 37.5V). The electrode is negatively biased so that the Si surface is in accumulation and the electric field is applied effectively. Applied electric field (or voltage) is measured when the oxide leakage current reaches a predetermined value (judgment current), in other words when the gate oxide breaks down. The influence of COPs on gate oxide breakdown can be estimated from the distribution of breakdown electric field.

7 Summary of Method

7.1 *Overview* — This test method consists of two parts. The first one is the fabrication of a number of similar MOS capacitors on silicon wafers, and the second one is the measurement of the electric charge injected just before the dielectric breakdown of the MOS capacitors. To measure the injected electric charge, the voltage applied to a MOS capacitor is controlled so that the current is kept constant. The voltage is monitored throughout the test, and the time from the beginning to a sudden voltage drop which results from the dielectric breakdown of the silicon dioxide film is measured. The injected electric charge is the product of the measured time and the gate current density.

7.2 *MOS Capacitor Fabrication Process* — Many MOS capacitors are formed on the test wafer. The MOS fabrication process consists of wafer cleaning, thermal oxidation, poly-Si deposition, phosphorous doping, activation heat treatment, photolithography and etching, in the case of using poly-Si electrodes. The details of the MOS capacitor fabrication process are shown in SEMI M51. When materials other than poly-silicon are used for electrodes, the process shall be adjusted to the material used. Although thermally grown 20 to 25 nm-thick gate oxide films are recommended in SEMI M51, oxide films as thin as 10 nm can be used depending on the situation. However, measurement shall be performed carefully for oxide films thinner than 3 nm, because breakdown judgment becomes difficult under the influence of direct tunneling current.

7.3 *Fabrication Environment* — It is necessary to fabricate MOS capacitors in a clean room environment of class 6 or better as indicated in ISO 1466-1. This means that, it needs to be confirmed that the A mode failure rate is 10% or less by TZDB evaluation. The A mode failure depends not only on the particle of work environment atmosphere but also on the ultrapure water, fixtures, process apparatus, clean clothes, operation rules etc. Heavily contamination such as alkaline or heavy metal has an important negative effect on the GOI of the oxide.

7.4 *Measurement of Electric Characteristic of MOS Capacitors*

7.4.1 The dielectric breakdown defect density of the silicon oxide film is evaluated by constant current TDDB measurement of the MOS capacitors. The evaluation consists of the measurement of charge injected before the dielectric breakdown of the MOS capacitors. To measure the injected charge, voltage applied to a MOS capacitor is controlled so that the current is kept constant. The applied voltage is monitored throughout the test, and the time to sudden voltage drop which results from dielectric breakdown of the silicon dioxide film is measured. The amount of the injected charge is the product of the measured time and gate current density. The defect density of the oxide film

SUPERSEDED

Documents
Document Sharing Hub
Full document details: SEMI M60-1113

is evaluated from the Weibull plot (cumulative failure rate) of the dielectric breakdown data of approximately 100 MOS capacitors.

7.4.2 *Stress Current Density* — For reliable measurement, a voltage/current source with a stable output wave shape shall be used. It is necessary to stabilize the output as much as possible. In the constant current TDDB measurement, a constant current is continuously applied, and voltage is monitored. The dielectric breakdown is judged by a sudden drop in the voltage monitored. If the applied stress current density is too low, the time to breakdown will be too long to be realistic. Contrarily, too a high current density is also unsuitable because the voltage drop in the oxide breakdown instant becomes small. Considering these factors, the recommended stress current density range is from 0.001 to 0.1 A/cm^2. The stress gate current has to be accumulated on the silicon surface.

7.5 *Measurement Temperature* — Besides current density, the measurement temperature is also an important parameter which determines measurement time. It is appropriate to measure in the temperature range of room temperature to 150°C, taking into consideration the temperature tolerance of the measurement equipment. In addition, there are cases that since silicon wafer, stage chuck, probe, and so on, expand at a high temperature, the probe deviates from the predetermined position, thus consideration is required when selecting probing machines.

7.6 *Breakdown Judgment* — To measure the dielectric breakdown lifetime of an oxide film, the voltage applied to a MOS capacitor is controlled so that a current is kept constant. The applied voltage is monitored throughout the test. The dielectric breakdown of the oxide is judged by sudden voltage drop. In practice, at the dielectric breakdown the applied voltage becomes lower than the criterion voltage defined before. The dielectric breakdown lifetime is the stress application time till breakdown. If the criterion voltage is too low, it can easily affected by noise. In contrast, the chance of missing breakdown events is increased if the criterion voltage is too high. The changes in two continuous measured gate voltages can be used to judge the oxide breakdown. The instant at which the voltage change became larger than the criterion value is defined as dielectric breakdown. The same caution mentioned above is also required in this case. In this round robin, the current density is from 0.001 to 0.1 A/cm^2, the sheet resistance of the poly-silicon electrode is approximately 50 ohm/sq, gate electrode area is from 1 mm^2 to 10 mm^2, gate oxide thickness is 25 nm and measurement temperature is from room temperature to 150°C. In this case dielectric breakdown is determined from the changes in two continuous measured gate voltages. For example, the change in gate voltage is larger than $X_{criterion}$(%) of the former gate voltage value. $X_{criterion}$ is higher than 10%. Alternatively, dielectric breakdown is determined with the measured electric field, E_{ox}. It is considered that dielectric breakdown does not happen until E_{ox} becomes $E_{criterion}$ or lower. $E_{criterion}$ is higher than 4 MV/cm. Stable measurement results are obtained in both cases. Of course, these criterion electric fields depend on gate oxide thickness, sheet resistance and area of gate electrode, stress current, stress temperature, and so on. To detect the dielectric breakdown with the change in gate voltage as shown in Figure 2, it is desirable to determine the criterion under each condition in advance.

7.7 *Estimation of Accidental Failure Rate* — As mentioned before, the total number of A-A and A-B mode failures is related to the crystal quality of the mirror polished CZ Si wafers. It takes a long time to measure the wearout lifetime of all the MOS capacitors. If a requirement is only measurement of the accidental failure rates of the MOS capacitors on silicon wafer surface, TDDB measurement can be finished without detecting the wearout lifetimes. That is, maximum stress time, T_{max}, is determined to be Q_{bd} in the A-B mode range in advance. The cumulative failure rate at T_{max} is the total failure rate of the A-A and A-B modes. If the rough shapes of the Weibull plots of the TDDB measurement can be predicted in advance, T_{max} shall be determined as to be the maximum Q_{bd} in the relatively flat range of the A-B mode. This reason is that variation of T_{max} has little influence on the evaluation of total accidental failure rates. This method has an advantage of that the failure rate of the A-A and A-B modes is evaluated very quickly.

7.8 *Constant-Voltage TDDB* — The constant-voltage TDDB method is also used for a lifetime test. Measurement conditions shall be optimized for each purpose. For TDDB, an average electric field of approximately 10 MV/cm is required. Therefore, the effective electric field applied to an oxide film is influenced by a series resistance. Thus, the constant current TDDB is more suitable.

SUPERSEDED

Documents Document Sharing Hub
Full document details: SEMI M60-1113