# SEMI M61-0612 (Reapproved 0319)
# SPECIFICATION FOR SILICON EPITAXIAL WAFERS WITH BURIED LAYERS

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on August 17, 2018. Available at www.semiviews.org and www.semi.org in March 2019; originally published July 2005; previously published June 2012.

## 1 Purpose

1.1 Some silicon epitaxial wafers are supplied with buried layers under the epitaxial film. This Specification covers the properties of such epitaxial wafers that pertain to the buried layer.

## 2 Scope

2.1 This Specification defines the properties of silicon epitaxial wafers with buried layers that relate to the characteristics of photolithography, buried layer, and buried layer pattern after the deposition of the epitaxial layer.

2.2 This Specification is intended to be used with the polished wafer specification (SEMI M1) and the epitaxial wafer specification (SEMI M2), which define the properties of the substrate and the epitaxial layer, respectively.

**NOTICE:** SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

## 3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M2 — Specification for Silicon Epitaxial Wafers for Discrete Device Applications

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M59 — Terminology for Silicon Technology

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

3.2 *ANSI Standard*[1]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *JEITA Standard*[2]

JEITA EM-3501 — Standard Methods for Determining the Orientation of a Semiconductor Silicon Single Crystal

**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

## 4 Terminology

4.1 General terminology for silicon wafers and silicon technology is covered in SEMI M59.

4.2 Terms related to epitaxial wafers with buried layers are as follows:

4.2.1 *alignment precision* — pattern displacement in first mask photolithography process.

4.2.2 *buried layer* — a diffused region in a substrate that is, or is intended to be, covered with an epitaxial layer.

[1] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, http://www.ansi.org

[2] Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; http://www.jeita.or.jp



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4.2.3 *pattern distortion ratio* — absolute magnitude of the quotient of (1) the difference between the width of the pattern on the substrate and the width of the pattern on the top surface of the epitaxial layer and (2) the thickness of the epitaxial layer.

4.2.4 *pattern shift ratio* — lateral distance between the center point of the pattern on the surface of the substrate and the center point of the pattern on the surface of the epitaxial layer divided by the epitaxial layer thickness.

4.2.5 *pattern step height* — difference in vertical position of the diffused (buried layer) surface and the original substrate surface, after removal of oxide.

## 5 Ordering Information

5.1 Purchase orders for silicon epitaxial wafers furnished to this Specification shall include the items indicated in sections 4-1 through 4-3 of Part 4 of the Specification Format for Order Entry (for Epitaxial Wafer with Buried Layer) shown in Table 1. Other specified characteristics, as required, may be added in section 4-4 of the format.

5.2 In addition, the purchase order shall include:

- the material in Part 1 (General Information) of the Specification Format for Order Entry, in SEMI M1,
- specifications for the substrate wafer of the appropriate characteristics as defined in Part 2 (Polished Wafer or Substrate) also in SEMI M1, and
- specifications for the epitaxial layer as defined in SEMI M2.

NOTE 1: Note that the orientation of single crystal is differently specified in SEMI MF26 and JEITA EM-3501.

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures.

5.3.2 Certification (if required).

5.3.3 Packing and marking requirements.

**Table 1 Specification Format for Order Entry**
**Part 4 Epitaxial Wafer with Buried Layer**

| *ITEM* | | *SPECIFICATION* |
|---|---|---|
| **4-1 PHOTOLITHOGRAPHY CHARACTERISTICS** | | |
| 4-1.1 | Mask ID | [ ] Number: [ ]; [ ]None |
| 4-1.2 | Alignment Precision | *X* max [ ] µm, *Y* max [ ] µm;<br>Reference Point (Wafer Coordinate System): *x* [ ] mm, *y* [ ] mm;<br>$\theta$ max [ ]° |
| 4-1.3 | Pattern Line Width Tolerance | Tolerance ± [ ] µm |
| **4-2 BURIED LAYER CHARACTERISTICS** | | |
| 4-2.1 | Dopant | [ ]B; [ ]P; [ ]Sb; [ ]As |
| 4-2.2 | Diffusion Depth ($x_j$) | Nominal [ ] ± Tolerance [ ] µm |
| 4-2.3 | Sheet Resistance | Nominal [ ] ± Tolerance [ ] Ω/sq |
| 4-2.4 | Pattern Step Height | Nominal [ ] ± Tolerance [ ] nm |
| 4-2.5 | Defect Density (Before Epi) | Not greater than [ ]/cm$^2$ |
| **4-3 BURIED LAYER PATTERN CHARACTERISTICS AFTER EPI** | | |
| 4-3.1 | Pattern Shift Ratio | Nominal [ ] ± Tolerance [ ] |
| 4-3.2 | Pattern Distortion Ratio | Max. [ ] |
| **4-4 OTHER CHARACTERISTICS** | | |
| | | |
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