SEMI M62-0514
SPECIFICATIONS FOR SILICON EPITAXIAL WAFERS

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NOTICE: This Standard replaced SEMI M2 and SEMI M11 in 2005.

SUPERSEDED

Contents

1 Purpose 2
2 Scope 2
3 Referenced Standards and Documents 3
4 Terminology 5
5 Ordering Information 5
6 Requirements 6
7 Specification Guides for IC Applications 13
8 Sampling 14
9 Test Methods 15
10 Certification 15
11 Product Labeling 16
12 Packing and Marking Shipping Container Labeling 16
RELATED INFORMATION 1 17
RELATED INFORMATION 2 19

List of Tables

Table 1 Silicon Wafer Specification Format for Order Entry, Part 3 Epitaxial Wafer 7
Table 2 Epitaxial Wafer Defect Limits 12
Table 3 Epitaxial Wafer Categories 13
Table R1-1 Number of Localized Light Scatterers in the Fixed Quality Area of Wafers of Different Sizes as a Function of LLS Density 17
Table R2-1 Guide for Specification of 1.0 µm, 0.35 µm, and 0.25 µm Design Rule Epitaxial Wafers 19
Table R2-2 Guide for the Specification of 0.18 µm Design Rule Epitaxial Wafers 21
Table R2-3 Guide for the Specification of 130 nm Design Rule Epitaxial Wafers 23
Table R2-4 Guide for the Specification of 90 nm Design Rule Epitaxial Wafers with DSP Substrates 25
Table R2-5 Guide for the Specification of 65 nm Design Rule Epitaxial Wafers with DSP Substrates 28
Table R2-6 Guide for the Specification of 45 nm Design Rule Epitaxial Wafers with DSP Substrates 31
Table R2-7 Guide for the Specification of 32 nm Design Rule Epitaxial Wafers with DSP Substrates 33
Table R2-8 Guide for the Specification of 22 nm Design Rule Epitaxial Wafers with DSP Substrates 36

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Full document details: SEMI M62-0514

1 Purpose

1.1 Epitaxial silicon wafers are utilized for many integrated circuits and discrete semiconductor devices. To permit common processing equipment to be used in multiple device fabrication lines, it is essential for the dimensions of epitaxial wafers to be standardized.

1.2 In addition, as technology advances to smaller and smaller dimensions for the elements of high density integrated circuits, it has become of interest to standardize additional properties of epitaxial wafers.

1.3 These specifications define and provide examples of silicon epitaxial wafer requirements for both discrete semiconductor device manufacture and integrated circuit device manufacture. By defining inspection procedures and acceptance criteria, both suppliers and their customers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 These specifications cover characteristics of both the substrate (through reference to SEMI M1) and the epitaxial layer, including handling and packaging.

2.1.1 The specification for epitaxial silicon wafers for discrete semiconductor device manufacture is specifically directed to silicon homoepitaxial deposits thicker than 25 µm on homogeneous silicon substrates or similar epitaxial wafers that are to be used to make discrete devices. For these wafers, device feature sizes are generally in excess of 1 µm.

2.1.1.1 The primary standardized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

2.1.1.2 Specific requirements for density of selected surface defects and variations of layer thickness and layer net carrier density are included together with AQLs for these properties.

2.1.1.3 In addition, Part 3 of the Silicon Wafer Specification Format for Order Entry,[1] which is included as Table 1, can be used to facilitate inclusion of such additional physical properties and suitable test methods as may be required in the specification.

2.1.2 The specifications for epitaxial silicon wafers for integrated circuit applications are restricted to wafers of diameter of 100 mm or greater with epitaxial layer thickness less than or equal to 25 µm.

2.1.2.1 These specifications are specifically directed to silicon homoepitaxial deposits on homogeneous silicon substrates only, for which more stringent uniformity and surface defect criteria are required than for epitaxial silicon wafers for discrete semiconductor applications.

2.1.2.2 The primary standardized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

2.1.2.3 Specific requirements for density of selected surface defects (Table 2) and variations of layer thickness and layer net carrier density are included together with AQLs for these properties. One type of such defect is localized light scatterers (LLS) such as particles, pits, and other surface defects. A table of equivalent LLS density per unit area and number of LLS within the fixed quality area of a wafer is provided in Related Information 1.

2.1.2.4 In addition, Part 3 of the Silicon Wafer Specification Format for Order Entry, which is included as Table 1, can be used to facilitate inclusion of such additional physical properties and suitable test methods as may be required in the specification.

2.1.2.5 Guides formed by a consensus of viewpoints are provided to suggest a foundation to specify an epitaxial wafer for use in integrated circuit manufacture at advanced design rules. Because these guides are not formal specifications but are suggestions from which a specification can evolve, they are provided in Related Information 2. The required specification is determined by the device and the process design. The usefulness of the guides can be increased by considering them prior to developing a device design or process.

[1] This table was formerly included in SEMI M18.

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2.2 The complete EDI Code List for items in the Order Form appropriate to silicon wafers, including epitaxial wafers, remains in SEMI M18.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M17 — Guide for a Universal Wafer Grid

SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M44 — Guide for Conversion Factors for Interstitial Oxygen in Silicon

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Reference Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI M59 — Terminology for Silicon Technology

SEMI M78 — Guide for Determining Nanotopography of Unpatterned Silicon Wafers for the 130 nm to 22 nm Generations in High Volume Manufacturing

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-Implanted Layers Using an In-Line Four-Point Probe with the Single-Configuration Procedure

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavenumber or Wavelength of the Plasma Resonance Minimum

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF525 — Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF723 — Practice for Conversion Between Resistivity and Dopant or Carrier Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Non-Contact Scanning

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SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Non-Contact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Non-Contact Scanning

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectrometry

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI Standards*[2]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/EIA 556-B — Outer Shipping Container Bar Code Label Standard

3.3 *DIN Standards*[3]

DIN 50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

DIN 50436 — Measurement of the Metallurgical Thickness of Epitaxial Layers of Silicon by the Stacking Fault Method

DIN 50437 — Measuring the Thickness of Silicon Epitaxial Layers by Infrared Interference Method

DIN 50439 — Determination of the Dopant Concentration Profile of Single Crystalline Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact

DIN 50441-3 — Measurement of the Geometric Dimensions of Semiconductor Slices; Determination of Flatness Deviation of Polished Slices by Means of Multiple Beam Interference

DIN 50443-1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-ray Topography: Silicon

DIN 50444 — Conversion between Resistivity and Dopant Density; Silicon

DIN 50447 — Contactless Determination of the Electrical Sheet Resistance of Semiconductor Layers with the Eddy-current Method

3.4 *European Community Directive*[4]

2002/95/EC — On the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment

3.5 *ISO Standards*[5]

ISO 14644-1 — Cleanrooms and Associated Controlled Environments – Part 1: Classification of Airborne Particulates

[2] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: 212.642.4900, Fax: 212.398.0023, http://www.ansi.org

[3] Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany; http://www.din.de

[4] *Official Journal of the European Union*, February 13, 2003 Available for downloading from the following URL: http://164.36.164.20/sustainability/pdfs/finalrohs.pdf

[5] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, http://www.iso.ch

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ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy (TXRF) on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy (TXRF)

3.6 *JEITA Standard*[6]

JEITA EM-3401 — Terminology of Silicon Wafer Flatness

3.7 *JIS Standards*[7]

JIS H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

JIS H 0611 — Methods of Measurement of Thickness, Taper, and Bow of Silicon Wafers

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms, acronyms, and symbols relating to silicon technology and epitaxial silicon technology are defined in SEMI M59.

5 Ordering Information

5.1 Purchase orders for epitaxial silicon wafers furnished to these specifications shall include the appropriate order entry information from Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, Table 1 in SEMI M1.

5.1.1 All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included:

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions
- 2-6.3 Primary Flat/Notch Orientation
- 2-6.4 Secondary flat length (or none)
- 2-6.5 Secondary flat location (or none)
- 2-6.6 Edge Profile
- 2-6.7 Thickness

5.1.2 Other items from Part 2, Polished Wafer or Substrate, can be included as needed.

5.1.3 In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist.

[6] Formerly JEIDA 43; Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; http://www.jeita.or.jp

[7] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: 81.3.3583.8005, Fax: 81.3.3586.2014, http://www.jsa.or.jp

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5.2 Purchase orders furnished to these specifications shall also include the items with a ♦ symbol in the left-most column of Table 1, Silicon Wafer Specification Format for Order Entry, Part 3. These are:

- 3-1.1 Conductivity Type/Structure
- 3-1.2 Layer Dopant
- 3-1.3 Silicon Source Gas
- 3-1.4 Layer Growth Method
- 3-1.5 Layer Net Carrier Density or Resistivity, center point
- 3-1.6 Net Carrier Density Variation
- 3-1.7 Layer Thickness, center point
- 3-1.8 Layer Thickness Variation

NOTE 1: The dopant, doping method, and growth method are difficult to ascertain in the finished wafers. Verification test procedures or certification of these characteristics should be agreed upon between the supplier and the customer (see § 9).

NOTE 2: Care should be taken in converting between carrier density and resistivity using SEMI MF723. Multiple conversions may introduce differences in values. For example, converting from carrier density (C_i) to resistivity and back to carrier density (C_f), may result in C_i not equaling C_f.

5.2.1 Also, appropriate epitaxial wafer defect limits from 3-4 and 3-5 of Part 3 shall be included. The importance of various defects may vary from application to application, but minimum requirements for defect limits for epitaxial wafers are given in Table 2.

5.2.2 Limits for slip, which may require destructive testing, shall be specified in the purchase order together with an appropriate test method.

5.2.3 Other items from Part 3, Epitaxial Wafer, can be included as needed.

5.2.4 In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist.

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures.

5.3.2 Certification (if required).

5.3.3 Packing and shipping container labeling requirements.

6 Requirements

6.1 As a minimum, the substrate shall conform to SEMI M1 and the appropriate substrate (polished wafer) category requirements (see Tables 5 through 11 in SEMI M1 for the requirements for various wafer categories).

6.2 If specified on the purchase order, the wafers shall conform to the Restriction of Hazardous Substances (RoHS) regulatory requirements of EC Directive 2002/95/EC. For information, the maximum concentrations of Cr, Cd, Hg, and Pb in the bulk or on the surface of the wafer required by this directive are given in SEMI M1.

6.3 Epitaxial wafer defects shall not exceed the limits given in Table 2. In this table, the defect limits (except for edge chips and indents) apply to the fixed quality area of the wafer except for any area included in a window where there is a laser identification mark.

6.3.1 In the absence of another specification, epitaxial wafers for IC applications shall contain no slip lines within the quality area.

NOTE 3: When an unetched wafer is observed for slip it is impossible to differentiate between slip and linear misfit lines.

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6.4 *Layer Thickness Variation*

6.4.1 *Epitaxial Wafer for Discrete Semiconductor Device Manufacture* — Unless otherwise specified, the thickness variation shall be determined from values measured at the center and half radius ($R/2$) locations, on diameters both parallel and perpendicular to the primary flat, and shall be ≤6% defined as follows:

$$\text{Variation (\%)} = \frac{\left(\frac{R}{2} - C\right)_{\max}}{C} \times 100 \tag{1}$$

where $\frac{R}{2}$ denotes one of the thickness values measured at half radius and C denotes the value at the center.

6.4.2 *Epitaxial Wafer for IC Applications* — Unless otherwise specified, the thickness variation shall be determined from value measured at the center and locations centered 12 mm ± 1 mm from the periphery, on diameters both parallel and perpendicular to the primary flat or notch axis, as follows:

$$\text{Variation (\%)} = \frac{t_{\max} - t_{\min}}{t_{\max} + t_{\min}} \times 100 \tag{2}$$

where $t_{\max}$ and $t_{\min}$ denote the maximum and minimum thickness values measured. The 12 mm locations have been defined based on instrument processing and fixturing considerations.

6.5 *Layer Net Carrier Density Variation*

NOTE 4: In many cases, this variation is described in terms of resistivity variation. It is possible to convert between resistivity and net carrier density with the use of SEMI MF723. However, it must be noted that the center point of a specification expressed in resistivity differs from that expressed in net carrier density. Consequently, the distributions may be skewed in different ways around the center point.

6.5.1 *Epitaxial Wafer for Discrete Semiconductor Device Manufacture* — The net carrier density variation shall be determined from values measured at the center and half radius ($R/2$) locations, on diameters both parallel and perpendicular to the primary flat, and shall be ≤10% for net carrier density ≥1×10^{15} cm^{-3} and ≤15% for net carrier density <1×10^{15} cm^{-3} defined as follows:

$$\text{Variation (\%)} = \frac{\left(\frac{R}{2} - C\right)_{\max}}{C} \times 100 \tag{3}$$

where $\frac{R}{2}$ denotes one of the net carrier density values measured at half radius and C denotes the value at the center.

Table 1 Silicon Wafer Specification Format for Order Entry, Part 3 Epitaxial Wafer

	ITEM		*SPECIFICATION*	*MEASUREMENT METHOD*
3-1. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice* ***must*** *be indicated in order to minimally specify an epitaxial silicon wafer.*				
	FOR EPITAXIAL WAFERS FOR IC APPLICATIONS, THE ITEMS LISTED IN THIS ENTIRE TABLE MAY BE SPECIFIED INDIVIDUALLY OR [ ]Specified according to Epitaxial Wafer Category 11.[ ] (see Tables R2-1 through R2-4 for epitaxial wafer categories). If the items are specified according to a standard category, none need be entered individually anywhere in this table unless (1) a choice must be made between various options in the category requirements or (2) an exception is desired.			
♦	3-1.1	Conductivity Type/Structure	[ ]n/n^+; [ ]p/p^-; [ ]p/p^+; [ ]p/p^{++}; [ ]Other: (specify)_____	
♦	3-1.2	Layer Dopant	[ ]Boron; [ ]Phosphorus; [ ]Arsenic	
♦	3-1.3	Silicon Source Gas	[ ]SiH_4; [ ]SiH_2Cl_2; [ ]$SiHCl_3$; [ ]$SiCl_4$;	
♦	3-1.4	Layer Growth Method	Reactor Type [ ]; Pressure [ ]	

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
♦	3-1.5	Layer Net Carrier Density or Resistivity, center point If Resistivity is Measured Convert to Net Carrier Density	Nominal [ ] ± Tolerance [ ] × $10^{[\ ]}$ atoms/cm^3 or Nominal [ ] ± Tolerance [ ] Ω·cm [ ]Yes; [ ]No	[ ]SEMI MF1392; [ ]DIN 50439; [ ]SEMI MF398; [ ]SEMI MF374; [ ]SEMI MF672; [ ]DIN 50447 [ ]Other: (specify)_____ [ ]SEMI MF723 [ ]DIN50444
♦	3-1.6	Net Carrier Density Variation Measurement Position and Calculation	[ ]≤10%; [ ]≤15%; [ ]≤____% [ ]Center and Half Radius (Equation 3); [ ]Center and 12 mm from edge (Equation 4); [ ]Other_____	[ ]SEMI MF1392; [ ]DIN 50439, [ ]Other: (specify)_____
♦	3-1.7	Layer Thickness, center point	Nominal [ ] ±Tolerance [ ] µm	[ ]SEMI MF95; [ ]DIN 50437; [ ]SEMI MF110; [ ]SEMI MF672; [ ]DIN 50436; [ ]Other: (specify)_____
♦	3-1.8	Layer Thickness Variation Measurement Position and Calculation	[ ]≤6%; [ ]≤____% [ ]Center and Half Radius (Equation 1); [ ]Center and 12 mm from edge (Equation 2); [ ]Other_____	Use same method as in 3-1.7 at each position
	3-1.9	Transition Width	[ ]≤_____µm	Use same methods as in 3-1.7 (IR only, for thickness measurement) and 3-1.10 (for carrier density measurement)
	3-1.10	Flat Zone	[ ]≤_____µm	[ ]SEMI MF1392; [ ]DIN 50439; [ ]Other: (specify)_____
	3-1.11	Phantom Layer	[ ]None	
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
	3-2.1	Bow	[ ]≤_____ µm	[ ]SEMI MF534; [ ]JIS H 0611; [ ]Other: (specify)_____
	3-2.2	Warp	[ ]≤_____ µm	[ ]SEMI MF657; [ ]SEMI MF1390; [ ]Other: (specify)_____
	3-2.3	Sori	[ ]≤_____ µm	[ ]SEMI MF1451; [ ]Other: (specify)_____
	3-2.4	Total Thickness Variation	[ ]TTV; [ ]GBIR; [ ]Other: (specify)_____	[ ]SEMI MF533; [ ]SEMI MF657; [ ]SEMI MF1530; [ ]JIS H 0611; [ ]DIN 50441/1; [ ]Other: (specify)_____
	3-2.5	Flatness, Global	[ ]≤_____ µm; Acronym[#1] [ ] [ ] [ ] [ ]	[ ]SEMI MF1530; [ ]DIN 50441/3; [ ]JEITA EM-3401; [ ]Other: (specify)_____
	3-2.6	Flatness, Site	[ ]≤_____ µm; Acronym[#1] [ ] [ ] [ ] [ ] Site Size ___ mm × ___ mm [ ]% Usable Area_____ [ ]Include partial sites; [ ]Do not include partial sites Offset: x = [ ] mm, y = [ ] mm	[ ]SEMI MF1530; [ ]Other: (specify)_____
	3-2.7	Nanotopography	[ ]≤___ nm for 2 mm diameter analysis area; and [ ]≤___ nm for 10 mm diameter analysis area; [ ]Other: (specify) _____	[ ]SEMI M43; [ ]Other: (specify)_____
	3-2.8	Misfit dislocations	[ ]to be determined	[ ]to be determined
	3-2.9	Flatness, Site, SBIR	[ ]to be determined	[ ]SEMI MF1530; [ ]Other: (specify)_____
	3-2.10	Edge Profile	[ ]to be determined	[ ]to be determined

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	3-2.11	Edge Roll Off	[ ]to be determined	[ ]to be determined
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
	3-3.1	Surface Metal Contamination		
	3-3.1.1	Sodium	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	3-3.1.2	Aluminum	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	3-3.1.3	Potassium	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.4	Chromium	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.5	Iron	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.6	Nickel	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.7	Copper	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.8	Zinc	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.9	Calcium	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2	Other Surface Metals (List Separately)		
	3-3.2.1	Cobalt	[ ]≤[ ] × $10^{[\ ]}$atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	3-3.2.2	Manganese	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.3	Molybdenum	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.4	Titanium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.5	Vanadium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.6	[ ]Other: (specify)_____	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
	THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY OR THEY MAY BE: [ ]Specified according to Table 2, Discrete Applications, or [ ]Specified according to Table 2, IC Applications. In either of these latter cases, individual listed items need not be entered individually in this section unless an exception is desired.			
	3-4.1	Stacking Faults	[ ]1/cm^2; [ ]Other: (specify)_____	[ ]SEMI MF1726; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.2	Slip	[ ]36 grid elements (Discrete Epitaxial Wafer only); [ ]None; [ ]Other: (specify)_____	[ ]SEMI M17 [ ]SEMI MF1726
	3-4.3	Dislocations	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF1726
	3-4.4	Large Localized Light Scatterers, Size >1 µm on side	[ ]None; Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.5	Localized Light Scatterers (LLS)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.6	Haze	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.7	Scratches – Macro	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
	3-4.8	Scratches – Micro	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.9	Edge Chips and Indents	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.10	Foreign Matter	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.11	Dimples	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.12	Orange Peel	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.13	Contamination/Area	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.14	Edge Cracks	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.15	Edge Crown	[ ]Projection above layer surface ≤1/3 of layer thickness; [ ]None; [ ]Other: (specify)_____	[ ]DIN 50446; [ ]Other: (specify)_____
	3-4.16	Cracks, Crow's Feet	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.17	Mounds	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.18	Saw Marks	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.19	Dopant Striation Rings	[ ]None; [ ] Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]DIN 50443/1; [ ]Other: (specify)_____
	3-4.20	Stains	[ ]None; [ ] Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]Other: (specify)_____
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
	THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY OR THEY MAY BE [ ]Specified according to Table 2, Discrete Applications, or [ ]Specified according to Table 2, IC Applications. In either of these latter cases, individual listed items need not be entered individually in this section unless an exception is desired.			
	3-5.1	Contamination	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]Other: (specify)_____
	3-5.2	Scratches – Macro	[ ]None; [ ]Other: (specify cum length)_____ mm	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-5.3	Scratches – Micro	[ ]None; [ ]Other: (specify cum length)_____ mm	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	3-5.4	Localized Light Scatterers (LLS)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;#2 [ ]Other: (specify)_____
	3-5.5	Edge Chips	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;#2 [ ]Other: (specify)_____
	3-5.6	Cracks, Crow's Feet	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;#2 [ ]Other: (specify)_____
	3-5.7	Saw Marks	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;#2 [ ]Other: (specify)_____
	3-5.8	Stains	[ ]None; [ ] Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]Other: (specify)_____
3-6. OTHER POST-EPI CHARACTERISTICS (as required)				

#1 Flatness Acronyms are defined in the Flatness Decision Tree in Appendix 1 of SEMI M1.

#2 In today's technology, it may be possible to inspect for some of these items using automated surface scanning inspection systems (SSIS). Such systems should be calibrated according to SEMI M53 using polystyrene latex spheres deposited in accordance with SEMI M58. Some indication of the defects separable by such instruments is provided in SEMI M35; however, a standard test procedure has yet to be developed. Application of automated inspection with the use of an SSIS must be agreed upon between supplier and customer.

Table 2 Epitaxial Wafer Defect Limits

Item	Characteristic	Maximum Limit#1				
		Discrete Applications				IC Applications
		$t_{epi} < 25\ \mu m$	$50 > t_{epi} \geq 25\ \mu m$	$100 > t_{epi} \geq 50\ \mu m$	$t_{epi} \geq 100\ \mu m$	
3-4.1	Stacking Faults	15 per cm^2				1 per cm^2
3-4.2	Slip	n = 36 grid elements (SEMI M17)				None
3-4.3	Dislocations	not specified				None
3-4.4	Large LLS, at ≥20 µm LSE	0.07 per cm^2	0.09 per cm^2	0.12 per cm^2	0.15 per cm^2	Not specified
3-4.5	Total LLS, at ≥0.5 µm LSE	0.20 per cm^2	0.24 per cm^2	0.27 per cm^2	0.30 per cm^2	0.20 per cm^2
3-4.6	Haze#2	None				None
3-4.7	Scratches – Macro#3	None				None
3-4.8	Scratches – Micro#3	None				None
3-4.9	Edge Chips and Indents#4	None				None
3-4.10	Foreign Matter#2	None				None
3-4.15	Edge Crown#5	Projection above wafer surface not to exceed $(1/3)_{tepi}$				Not specified
3-5.1	Back Surface Contamination#2	None				None

#1 Except for edge chips and indents, defect limits apply to the fixed quality area of the wafer except for any area included in a window where there is a laser identification mark. Nominal edge exclusion is 4 mm for 150 mm wafers, 4, 3, or 2 mm for 200 mm wafers, and 3, 2, or 1 mm for 300 mm wafers.

#2 Any adherent contaminants, such as stains, glovemarks, dirt, smudges, warps, and solvent residues. This characteristic does not include point defects. Any nonadherent contamination or particulate matter easily removed by industry-accepted cleaning techniques shall not constitute foreign matter or haze.

#3 The cumulative AQL for both front surface and back surface of wafer is 2.5.

#4 The cumulative AQL for both front surface and back surface of wafer is 1.0.

#5 Edge crowning may be reduced by pre-epitaxy edge rounding or removed by post-epitaxy edge rounding.

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