SEMI M66-1110 (Reapproved 1121)
TEST METHOD TO EXTRACT EFFECTIVE WORK FUNCTION IN OXIDE AND HIGH-κ GATE STACKS USING THE MIS FLAT BAND VOLTAGE-INSULATOR THICKNESS TECHNIQUE

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1 Purpose

1.1 Continued scaling of CMOS integrated circuit dimensions is reaching a point where materials changes as well as lithographic advances are required to meet the projections of Moore's Law and the International Technology Roadmap for Semiconductors. As gate dielectric thickness approaches 1 nm, both the gate dielectric and electrode materials that have been in common usage—SiO_2, and doped polysilicon—are displaying characteristics that are unacceptable for upcoming technology nodes. Research to find suitable replacements for the n^+ and p^+ polysilicon gate electrodes used in conventional CMOS is placing renewed emphasis on experimental determination of the effective gate electrode work function of candidate materials.

1.2 One aspect of the research for new gate electrode materials is that they may be required for use on either silicon dioxide (SiO_2) gate dielectrics or on the high-κ gate dielectrics that are being developed to replace SiO_2. While it might seem that gate electrode work function differences should depend only upon the properties of the gate electrode material and the silicon substrate, it has been shown that various metal-dielectric interactions may cause potential shifts that affect the effective work function. Thus consideration must be given to structures and analyses that properly take these effects into account.

1.3 Changes in process technology and wafer fabrication practice since these measurements were first widely used suggest a need for revised approaches to test structure fabrication and analysis. Definition of such changes is the purpose of this Test Method, which covers the measurement, analysis and reporting of effective gate electrode work function data by the flat band voltage-insulator thickness technique.

2 Scope

2.1 This Test Method covers determination of the effective work function of both oxide and high-κ gate stacks. While the basic technique is based upon the conventional MOS capacitor flat band voltage-dielectric thickness approach as outlined in SEMI MF1153, two features of the present test method are keys to its usefulness: (1) the ability to provide a demonstrably good estimate of effective work function from measurements on a single silicon wafer, and (2) the ability to separate and minimize the effects of interfacial and bulk charge distributions in a high-κ gate stack on the effective work function value. Both of these features depend upon the nature and fabrication of the test structures used for the test method. The nature of the samples is so important to the application of the method that the terraced oxide technique, an automated approach to fabrication of suitable test structures using standard tools available in modern wafer fabs, is outlined as part of the test method and alternative, but probably less accurate and less reproducible, approaches suitable for use in smaller facilities are outlined in Related Information 1.

2.1.1 The use of a single silicon wafer that includes a range of dielectric thicknesses is the first key feature of this Test Method. This requirement was a standard feature of early measurements of effective work function by this technique, based on the convenience of etching a thermally grown oxide manually, by dipping it partially into a wet etchant. This approach maintains the validity of the procedure by assuring a uniform oxide-silicon interface charge

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density, for all test specimens included in the evaluation. The importance of this feature is seen in the basic expression underlying the analysis,

$$V_{fb} = \Phi'_{ms} - \frac{Q_f W_{ox}}{\varepsilon_{ox}} \tag{1}$$

where:

V_{fb} = flat band voltage (V),

Φ'_{ms} = potential barrier difference between the Fermi level in the gate electrode and the Fermi level in the silicon substrate (see ¶ 5.3.1) (V),

Q_f = oxide interface charge density (C/cm^2),

W_{ox} = oxide layer thickness (cm)[1], and

ε_{ox} = dielectric permittivity of the oxide (3.4×10^{-13} F/cm).

Equation 1 establishes that all the capacitors with varying oxide thickness must have the same value of Q_f to evaluate the gate electrode-silicon work function difference Φ'_{ms} by plotting the flat band voltage V_{fb} against the varying oxide thickness W_{ox}. Φ'_{ms} is used with the known work function of the silicon substrate to obtain the desired effective work function of the gate electrode material under investigation. Difficulty in building wafers in a modern wafer fab by varying the oxide thickness in a controlled fashion has led to the use of different wafers with fixed thicknesses for these experiments. Such samples may well have differing values of Q_f because of differing oxidation temperatures, ambients, or times. This is even more likely to be the case for high-κ gate stacks, with their differing deposition conditions. Thus, this test method stresses the use of single wafers with varying oxide thicknesses for extracting effective work function.

2.1.2 This Test Method specifically covers the extraction of effective work function for gate electrodes on high-κ gate stacks. The interaction of certain electrodes with high-κ dielectric surfaces can cause work functions to vary, depending upon the surface upon which the electrode is placed. The analysis can be simplified considerably by using high-κ gate stack structures in which a fixed thickness of the high-κ film is placed over the varying oxide thickness on a single wafer. In this case, charge distributions associated with the high-κ film and its interface with the oxide will affect the ordinate intercept of the V_{fb}–W_{ox} plot, interfering with the determination of Φ'_{ms}. This interference can often be reduced to negligible levels by using thin high-κ films. Where necessary, the magnitude of the fixed shift in the ordinate intercept can be evaluated by using multiple wafers with varying high-κ film thicknesses (see Related Information 2).

2.2 This Test Method requires the measurement of many MIS capacitance-voltage (C-V) curves, and extraction of the flat band voltage and equivalent oxide thickness (EOT) from this data. These C-V curves are high frequency C-V curves, typically measured at frequencies ranging from 100 kHz to 1 MHz. Accurate measurements of such C-V curves, particularly on relatively thin oxides or high-κ gate stacks, have many potential complications, the description of which is not included in SEMI MF1153, which covers measurements on oxides ≥50 nm thick, and is also beyond the scope of this Test Method.[2,3]

2.3 Extraction of values of V_{fb} and EOT from the C-V data taken here is an important part of the procedure. In the work shown herein, the CVC algorithm[2] developed by NCSU has been used. This is not critical to the analysis. Any consistent algorithm for this purpose may be used with the data.

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[1] This quantity is generally given in nm, in which case the value should be multiplied by 10^{-7} before using it in Equation 1.

[2] High frequency MOS C-V measurement theory and techniques are described in Schroder, D. K. *Semiconductor Material and Device Characterization*, John Wiley & Sons, Inc., 1990, Chapter 6, p. 244*ff*. Nicollian, E. H. and Brews, J. R., (*MOS (Metal Oxide Semiconductor) Physics and Technology*, John Wiley & Sons, Inc., 1982, Chapter 4, p. 99*ff* and Chapter 12, p. 581*ff*.

[3] Hauser, J. R. and Ahmed, K. "Characterization of Ultra-Thin Oxides Using Electrical C-V and I-V Measurements." in *Characterization and Metrology for ULSI Technology*, Seiler, D.G., *et al*. ed., AIP Conference Proceedings 449, American Institute of Physics (1998): pp. 235–239.

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3 Limitations

3.1 Since both the dielectric capacitance and flat band voltage are sensitive to series resistance, care must be taken to make sure that the wafer has a low resistance ohmic return contact. This is preferably done with a metallized contact to the back surface of the wafer under test. When testing must be done on capacitors in diffused wells of a conductivity type opposite to the substrate, top surface contacts carefully designed to provide uniform, low resistance to all parts of the test capacitor should be used.

3.2 A primary limitation of the terraced oxide technique is that it uses relatively thick thermal oxide as the dielectric for oxide-only applications or as the interfacial oxide in high-κ gate stack embodiments. Thus if nitrided oxides are to be used, the nitridation must be done to the thickest oxide before terrace etching, which may produce an interface unlike that which would be found when nitriding thinner oxides. Attempts to nitride the oxide after terrace etching result in non-uniform Q_f for the various oxide thicknesses, destroying the basic assumption underlying the analysis as discussed relative to Equation 1. For that matter, any thermal or active process applied to the terraced oxide after its formation may cause the same problem. For example, attempting to dry-etch the terraces causes nonuniform Q_f due to the plasma damage of the oxide-silicon interface. This concern also extends to damage associated with the deposition of the desired gate electrode material. If such damage does occur, it is easily detected in the early stages of data analysis.

3.3 Invalid or inapplicable data may result from C-V measurements of defective capacitors. Defects may arise from intrinsic or extrinsic defects in the dielectric, patterning errors in the electrode formation, or a formation across a transition between terraces. Therefore, it is essential that invalid data must be removed from the dataset before further analysis. This is best done by vetting the parameters extracted from the C-V analysis against the theoretical model from which the EOT and V_{fb} values are extracted. A check of the output parameters of the C-V data analysis algorithm is also advisable; for example, ensuring that all the calculated surface doping densities are tightly grouped and are the right magnitude.

3.4 The volume of data required for complete analysis may become very large; the original algorithm measured 128 MOS capacitors per wafer, each with about 100 data points. A semi-automated, computer-controlled prober and data acquisition system is advisable.

3.5 Consideration should be given to choosing silicon substrate doping levels with regard to the thickness or specific capacitance of the gate dielectrics to be used. The goal is to achieve a moderate C-V curve shape with the flat band capacitance near the center of the C-V transition for easy resolution of V_{fb}.

3.6 Care must be taken to ensure that the test wafer fabrication process adequately mirrors that envisioned for use in the processing of the gate electrodes in a completed device. Higher temperature anneals used for device implant activation are well-known sources of variation in gate electrode effective work functions. Neglect of proper low temperature anneals, particularly those in reducing ambients, may lead to high, variable interface state densities that distort the measured C-V characteristics and complicate the extraction of effective work function values. Distortions of the C-V curves due to gate electrode deposition process damage not only gives misleading work function values but also implies a serious problem in the use of this process for gate electrode deposition. The actual values of the effective work function obtained depend somewhat on the processing involved in fabricating the test structure. Care must be taken to ensure consistent processing.

3.7 When testing very thin oxides, 10 nm or less, special care must be taken to account for effects arising from the very high specific capacitance of these films. These may include voltage drops across the gate electrode if it is not highly conductive and the silicon substrate. High levels of conduction due to direct tunneling in these thin dielectrics may distort the C-V characteristics, complicating the analysis and parameter extraction.

4 Referenced Standards and Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI M59 — Terminology for Silicon Technology

SEMI MF1153 — Test Method for Characterization of Metal-Oxide-Silicon (MOS) Structures by Capacitance-Voltage Measurements

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5 Terminology

5.1 Acronyms, terms, and symbols related to silicon technology, including those used in this Test Method, are listed and defined in SEMI M59.

5.2 *Terminology Used in this Standard*

5.2.1 *effective work function* — the potential difference between the free space reference and the Fermi energy in the gate electrode of the gate stack of a CMOS device.

5.2.1.1 *Discussion* — The term 'work function' has a well-defined meaning in physics as the energy required to move an electron from thermal equilibrium at the surface of a material to free space external to the material. When the material is put in intimate contact with a dielectric film on a semiconductor surface to form the gate stack of a CMOS device, charge transfer takes place that is a function of various properties and interactions with these other materials that may affect the potential difference between the gate material and the substrate. Thus the final potential difference that is established and that controls the threshold voltage of the CMOS device may well be different from the difference in conventional work functions of the gate material and semiconductor substrate. Therefore the term 'effective work function' is used to express the value associated with the potential difference observed in the actual gate stack.

5.2.2 *terraced oxide wafer* — oxidized wafers that have been etched using an automated spin etcher so that a range of varying oxide thicknesses is created.

5.2.2.1 *Discussion* — These wafers are a key component of this test method in that they provide the needed set of MOS capacitors with varying oxide thicknesses, all on the same wafer, and with a common, uniform value of oxide-silicon interface charge, Q_f. To assure this latter property, a single thermal oxidation of the wafer must be done, followed by a benign oxide etch with a wet chemical etchant to prevent oxide-thickness-dependent interface charge generation.

5.3 *Symbols Used in this Standard*

5.3.1 Φ'_{ms} — potential barrier difference between the Fermi level in the gate electrode material and the Fermi level in the silicon substrate in an MIS capacitor structure.

5.3.1.1 *Discussion* — This potential difference is the ordinate intercept in a plot of flat band voltage, V_{fb}, and oxide thickness, W_{ox}, in a simple oxide-only test specimen. In the case of a high-κ gate stack, see ¶ 5.3.2.1.

5.3.2 Φ_i — ordinate intercept of a V_{fb}–W_{ox} plot for a test specimen incorporating a high-κ gate stack dielectric.

5.3.2.1 *Discussion* — In the case of the high-κ gate stack dielectric, the ordinate intercept includes the Φ'_{ms} of the gate electrode-silicon substrate plus terms involving bulk and interface charge and dipoles in the gate stack, but use of very thin high-dielectric films minimizes the difference (see Related Information 2).

6 Summary of Test Method

6.1 The test method begins with the proper preparation of test specimens and test structures.

6.2 The test specimen ID and other test identity are recorded.

6.3 The test parameters relevant to the test system and to the test specimens are established. These include parameters needed for the fabrication of the MOS capacitors to be tested, the definition of measurement conditions for the C-V curves to be measured, and the data that must be extracted for the analysis.

6.4 High frequency MOS C-V measurements are made on a small number of capacitors on each of the die on the wafer over which oxide thickness varies. Adequate provision must be made for zeroing out stray capacitance in all of these measurements. All C-V measurement data must be stored along with identification of the die from which they came and the area of the capacitor within that die.

6.5 When all capacitors specified for testing have been measured, the C-V data are processed through an algorithm for deriving appropriate parameters, including EOT, surface dopant density, flat band voltage, and a goodness-of-fit parameter indicating how well the data agree with the characteristics of a normal MOS capacitor with these parameters. The NCSU CVC algorithm is one such program for performing this analysis.[2]

6.6 Plots of V_{fb} versus EOT are formed from all the data from each wafer. These plots are analyzed by linear regression techniques to determine their linearity and hence the degree to which they meet the assumptions of the analysis

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outlined in the model derivation given in Related Information 2. If they meet linearity requirements, values of oxide-silicon interface charge Q_f and ordinate intercept values Φ'_{ms} or Φ_i are extracted.

6.7 The values of Φ'_{ms} or Φ_i determined for each wafer are used to derive effective work function values for their gate electrode materials.

6.8 If suitable data linearity is not found in the V_{fb} vs. EOT plots, the experiment must be analyzed to determine the source of the problem. The nature of this analysis depends upon the specific details of the experiment and cannot be adequately described here.

6.9 If variable thickness interfacial oxide/fixed thickness high-κ gate stacks are employed, it may be necessary to analyze wafers with varying thicknesses of the high-κ film on identically prepared terraced oxide substrates to separate and evaluate the effects of charges associated with the high-κ films and its interface on the effective work function of the gate electrode under test. This is described more fully in Related Information 2.

7 Apparatus

7.1 *Wafer Probing* — The use of computer-controlled probing equipment is essential as the measurement speed precludes manual data gathering. What is included here must be considered a minimum.

7.1.1 *LCR Meter/C-V Analyzer* — Capable of measuring capacitance at frequencies between 10 kHz and 1 MHz over a bias sweep range of +5 V to 5 V, at least. Good tolerance of high dielectric loss samples is important for thin dielectric samples. Computer control of all measurement parameters, data storage, and synchronization with the semi-automated probe station is mandatory.

7.1.2 *Semi-Automated Wafer Shielded Probe Station/Chuck* — This probe station must be adequately light and ambient-shielded for MOS C-V measurements and capable of automated probing from capacitor to capacitor within a die and from die to die.

7.2 *Wafer Processing* — Equipment for producing die with capacitors of various active areas with a gate oxide thickness of 10 nm, located in an ISO Class 5 or better as appropriate for the geometry being fabricated. All appropriate processing chemicals, test specimen holders, and necessary venting are required.

7.3 *Spin Etch Processor* — An instrument to form the terraced oxide structure, which spins the wafer horizontally while the etchant is dispensed downward through a tube or tubes aligned vertically and radially scanned. Specification of the initial thermally grown oxide thickness, the oxide etchant composition, the number and position of the etchant dispense tube positions, and the timing of their movement should control all physical parameters of the terraced oxide structure. This equipment should be capable of producing very reproducible terraced oxides (see ¶ 9.1.8).

NOTE 1: Alternative equipment, as described in Related Information 1, is required if the alternative procedures described there are used to form the test specimens.

8 Sampling

8.1 There are generally more devices on the test specimen than need to be measured. The number and nature of the test specimens to be examined in this test method shall be agreed upon between parties to the test.

8.2 Furthermore, because the values obtained cannot be entirely divorced from the process of fabricating the test structure, suitable correlations should be performed based on process needs and structure selection. This correlation should include test specimen size as well as device geometry.

9 Test Specimens

9.1 A central feature of this test method is the use of a single silicon wafer for all electrical measurements leading to the determination of the required gate electrode effective work function. With careful processing, this provides a constant oxide-silicon interface charge density for all samples independent of the varying EOT's, assuring the validity of assumptions underlying the analysis. The preferred method for preparing test specimens is the following automated terraced oxide test specimen approach that provides a test wafer made up of an array of test die, each incorporating MOS capacitors of varying area isolated by surrounding field insulator regions upon which probe pads are placed.

NOTE 2: Alternative approaches to the fabrication of such samples are included in Related Information 1.

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9.1.1 Before preparing the test specimens, establish the relevant test specimen parameters for fabrication and testing. Table 1 lists a typical set of such parameters.

9.1.2 First, process the wafers normally through active area definition, isolation oxide processing, and gate oxide formation to a thickness of 10 nm.

9.1.3 Then carry out a benign wet process etching of the initial thermally grown gate or interfacial oxide, done using a commercially available spin-spray etching tool to produce a radially symmetric annular pattern of varying oxide thickness across the wafer as pictured in Figure 1. The radially symmetric pattern contains a central thickest region surrounded by three annular regions, all of approximately equal area, forming a tiered or terraced structure reminiscent of a wedding cake. This figure shows thicknesses of 8, 6, 4, and 2 nm, although both thinner and thicker structures can be used. Control all of the physical parameters of the terraced oxide structure by specifying the initial thermally grown oxide thickness, the oxide etchant composition, the number and position of the etchant dispense tube positions, and the timing of their movement.

NOTE 3: For this baseline 2-4-6-8 nm process, a 10 nm thermally grown oxide is employed with an etchant composed by 5:1 dilution of concentrated hydrofluoric acid. For uniformity, it is important that all parts of the oxide surface be exposed to the etchant, so etching the entire oxide from 10 to 8 nm before terracing the rest of the oxidized wafer is the first step in the process.

Table 1 Test Specimen Parameters

Parameter Name	*Parameter Description*	*Reference Value*
	Silicon wafer conductivity type	*p*-type
	Silicon wafer resistivity (Ω·cm)	0.06 Ω·cm
n_t	Number of oxide terraces per wafer	4
$t_{ox}(1)$ to $t_{ox}(n_t)$	Oxide thickness for each terrace (nm)	8, 6, 4, and 2 nm
$r(1)$ to $r(\mathrm{I})$	Radii of oxide terraces (mm)	40, 60, 80, and 100 mm
t_{hk}	Thickness of high-κ film (nm)	2.5nm
$№_c$	Number of capacitors per wafer to be tested	128
$№_A$	Number of different capacitor areas	4
$A(1)$ to $A(№_A)$	Areas of the capacitors to be tested	5×10^{-5}, 1×10^{-4}, 2×10^{-4}, and 5×10^{-4}, cm^2

#1 This figure shows a thick isolation oxide patterned so that the thickness variation is visible in the varying color fringes associated with oxide thicknesses of 530, 480, 420, and 370 nm. In actual practice, the oxide to be etched is only of the order of 10 nm thick, the effect on the isolation oxide surrounding the gate dielectric active regions is negligible, and invisible to the naked eye.

Figure 1
Terraced Oxide Pattern Etched onto a 200 mm Diameter Wafer

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