

SEMI M67-0720

TEST METHOD FOR DETERMINING WAFER NEAR-EDGE GEOMETRY FROM A MEASURED THICKNESS DATA ARRAY USING THE ESFQR, ESFQD AND ESBIR METRICS

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on January 30, 2020. Available at www.semiviews.org and www.semi.org in July 2020; originally published November 2006; previously published October 2015.

1 Purpose

- 1.1 Wafer near-edge geometry can significantly affect the yield of semiconductor device processing.
- 1.2 Knowledge of near-edge geometrical properties can help the producer and consumer determine if the dimensional characteristics of a wafer satisfy given geometrical requirements.
- 1.3 This Test Method is suitable for quantifying the flatness aspects of near-edge geometry of wafers used in semiconductor device processing.
- 1.4 The ESFQR, ESFQD or ESBIR metric may be more suitable for quantifying the flatness aspects of near-edge geometry than traditional metrics such as SFQR, SFQD or SBIR. ESFQR, ESFQD and ESBIR quantify near-edge geometry fully and consistently at all angular positions on the wafer edge except at locations intentionally excluded. SFQR, SFQD and SBIR, on the other hand treat different angular positions differently and do not typically provide full coverage of the wafer edge.

NOTE 1: Acronyms beginning with E are analogous to those in Appendix 1 of SEMI M1 but relate to the near-edge region. The letter 'S' in these acronyms refers to an edge Sector rather than to an exposure Site.

- 1.5 Consideration should be given to the use of near-edge geometry metrics as a process control tool rather than a material exchange specification.
- 1.6 There are other metrics for near-edge geometry, some of which quantify other aspects such as ZDD, ROA and PSFQR.

NOTE 2: ERO is frequently employed as a more general term for describing near-edge geometry, but as of the approval date of this standard there are no standardized conditions or test procedures for it. As such a general term, ERO is included in the keywords for this standard, even though it is outside the scope of the Standard.

2 Scope

- 2.1 This Test Method covers calculation of the near-edge geometry metrics ESFQR, ESFQD and ESBIR.¹
- 2.2 The metrics calculated by this Test Method are based on a thickness data array. This array represents the front surface of the wafer when the back surface of the wafer is ideally flat, as when pulled down onto an ideally clean flat chuck.
- 2.3 This Test Method is suitable for polished, epitaxial, SOI, or other layer condition.
- 2.4 This Test Method is applicable to categories of wafers specified in SEMI M1 used in advanced IC manufacturing.
- 2.5 This Test Method does not cover acquisition of the thickness data array. However, it gives the required characteristics of the thickness data array.
- 2.6 Other metrics analogous to flatness metrics can be calculated, but these are outside the scope of this Test Method.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

¹ The calculation of these metrics is the subject of U.S. Patent 7,324,917 owned by KLA-Tencor Corporation, One Technology Drive, Milpitas, CA 95035. KLA-Tencor has informed SEMI that, per SEMI regulations, it will license this patent on reasonable and customary terms.

3 Limitations

- 3.1 Deficiencies of data such as inadequate spatial resolution, mispositioning, noise, etc. in the thickness data array used to calculate the metrics may lead to erroneous results.
- 3.2 The calculations of this Test Method do not remove wafer shape and therefore are not applicable to data obtained from unclamped wafer single-surface data.
- 3.3 The reference plane used in the calculation is dependent on both the radial length and sector span.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M59 — Terminology for Silicon Technology

SEMI M68 — Practice for Determining Wafer Near-Edge Geometry from a Measured Height Data Array Using a Curvature Metric, ZDD

SEMI M70 — Practice for Determining Wafer-Near-Edge Geometry Using Partial Wafer Site Flatness

SEMI M77 — Practice for Determining Wafer Near-Edge Geometry Using Roll-Off Amount, ROA

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI T7 — Specification for Back Surface Marking of Double-sided Polished Wafers with Two-dimensional Matrix Code Symbol

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Most acronyms, terms, and symbols used in silicon wafer technology, including those in this Test Method, are given in SEMI M59.

5.2 Definitions

5.2.1 *exclusion window* — an area on the wafer front or back surface that intersects the FQA from which acquired data, if any, are not used to calculate metrics.

NOTE 3: Exclusion windows may be used when: a) wafer suppliers and buyers agree to exempt certain areas in the vicinity of mandated features, such as notches and laser scribes, that affect metrics; b) a given measurement system's design precludes valid data acquisition, such as portions of the edge obscured by mechanical fixtures in the vicinity.

6 Summary of Test Method

6.1 Sectors for metric calculation are defined by FQA radius, sector radial length and sector angular extent. Required exclusions are defined (see § 7).

6.2 A thickness data array in an annulus of defined radial length and location is acquired.

6.3 A reference plane is constructed in each sector.

6.4 ESFQR for each sector is calculated as the range of the reference plane deviation within the sector.

6.5 ESFQD for each sector is calculated as the reference plane deviation having the largest absolute value within the sector while retaining the sign.

6.6 ESBIR for each sector is calculated as the range of thickness values within the sector.

6.7 Recipe parameters are reported.

6.8 ESFQR, ESFQD and ESBIR are reported for each sector. Statistical quantities for these parameters are also calculated and reported for each wafer.

7 Exclusion Windows

7.1 The area to be excluded are in the vicinity of:

- Wafer identification marks (alphanumeric and/or SEMI T7)
- Inscribed fiducial marks for 450 mm notchless wafers
- Fiducial notch
- Wafer handling contacts
- Other areas as may be agreed to by equipment suppliers, wafer suppliers, and customers

7.2 The position and the minimum size of the area for wafer identification marks, inscribed fiducial marks and fiducial notch are as specified in the relevant identification mark or wafer specification (see SEMI T7, SEMI M1, SEMI M12, SEMI M13).

7.3 The position and the actual size of exclusion windows, may include allowance for system-specific tolerances.

7.3.1 Definition of area exclusions in a polar coordinate system (see Figure 1).

7.3.1.1 Four parameters are defining the size and position of the area exclusion.

7.3.1.1.1 Angular position defined as θ_c representing the centered Theta position of the area exclusion.

7.3.1.1.2 Angular span as defined as $\Delta\theta$ representing the Theta extend of the area exclusion.

7.3.1.1.3 Inner radius defined as r_{min} representing the inner radial boundary position of the area exclusion.

7.3.1.1.4 Outer radius defined as r_{max} representing the outer radial boundary position of the area exclusion.

7.3.2 Definition of area exclusions in a Cartesian coordinate system (see Figure 2).

7.3.2.1 Four parameters are defining the size and position of the area exclusion.

7.3.2.1.1 Minimal horizontal boundary position as defined as X_{min} .

7.3.2.1.2 Maximal horizontal boundary position as defined as X_{max} .

7.3.2.1.3 Minimal vertical boundary position as defined as Y_{min} .

7.3.2.1.4 Maximal vertical boundary position as defined as Y_{max} .

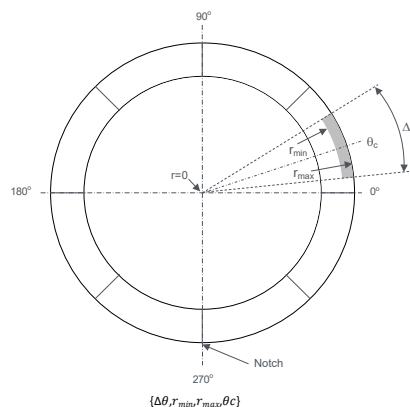


Figure 1
Polar Coordinate System for Wafer Handling Contacts and Fiducials