

SEMI M70-1108

PRACTICE FOR DETERMINING WAFER-NEAR-EDGE GEOMETRY USING PARTIAL WAFER SITE FLATNESS

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1 Purpose

- 1.1 Wafer near edge geometry can significantly affect the yield of semiconductor device processing.
- 1.2 Knowledge of near edge geometrical properties can help the producer and consumer to determine if the dimensional characteristics of a wafer satisfy given geometrical requirements.
- 1.3 This practice is suitable quantifying the near edge geometry of wafers used in semiconductor device processing.
- 1.4 The PSFQR or PSFQD metric is suitable for quantifying near edge geometry when applying a site pattern that appropriately covers large parts of the wafer edge.

NOTE 1: Acronyms beginning with P are the same as those in Appendix 1 of SEMI M1 except that they relate to the partial sites covering the near edge region.

1.5 Flatness metric is well-established therefore partial site flatness can be used as a process control tool as well as a material exchange specification for edge geometry.

1.6 There are other metrics i.e., ZDD, ESFQR, ROA, some of which quantify more specific aspects of edge geometry.

NOTE 2: ERO is frequently employed as a more general term for describing near edge geometry, but as of the approval date of this standard there are no standardized conditions or test procedures for it. As such a general term, ERO is included in the keywords for this standard, even though it is outside the scope of the standard.

2 Scope

2.1 This practice covers calculation of the near edge geometry metrics PSFQR and PSFQD.

2.2 SFQR and SFQD are well known parameters and described in detailed in SEMI MF1530. In contrast to SEMI MF1530 the present practice is dealing exclusively with the non-full sites (i.e., the partial sites). The practice is focused only and specifically on near edge geometry applications.

2.3 The metrics calculated by this practice are based on a thickness data array (see also SEMI MF1530). This array represents the front surface of the wafer when the back surface of the wafer is ideally flat, as when pulled down onto an ideally clean flat chuck.

2.4 This practice is suitable for polished, epitaxial, SOI, or other layer condition.

2.5 The practice is applicable to notched 200 and 300 mm diameter wafers having dimensions in accordance with wafer categories 1.9.2 and 1.15 of SEMI M1.

2.6 This practice does not cover acquisition of the thickness data array. However, it gives the required characteristics of the thickness data array.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Deficiencies of data such as inadequate spatial resolution, mis-positioning, noise, etc. in the thickness data array used to calculate the metrics may lead to erroneous results.

3.2 The calculations of this practice do not remove wafer shape and therefore are not applicable to data obtained from unclamped wafer single-surface data.

3.3 The reference plane used in the calculation is dependent on the x - and y -length of the sites and the x - and y -offset of the site pattern.

4 Referenced Standards and Documents

4.1 SEMI Standards

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M49 — Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 22 nm Technology Generations

SEMI M59 — Terminology for Silicon Technology

SEMI M67 — Practice for Determining Wafer Near-Edge Geometry from a Measured Thickness Data Array Using the ESFQR and ESFQD Metrics

SEMI M68 — Practice for Determining Wafer Near-Edge Geometry from a Measured Height Data Array Using a Curvature Metric, ZDD

SEMI M69 (Preliminary) — Practice for Determining Wafer Near-Edge Geometry Using Roll-Off Amount, ROA

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Non-Contact Scanning

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Many terms used in silicon wafer technology are defined in SEMI M59.

5.2 Other Definitions

5.2.1 *edge roll off (ERO)* — surface deviations of a large-diameter silicon wafer near the edge, but excluding effects due to wafer edge profiling and surface roughness.

5.2.2 *near edge geometry* — the topography of a surface of a large diameter silicon wafer in the outer region of the fixed quality area (FQA).

5.2.3 *partial site* — a site as defined in SEMI M59 but with some of its area outside the FQA.

5.2.4 *ESFQR* — near-edge silicon wafer geometry flatness metric similar to SFQR (see Appendix 1 of SEMI M1) that relates to the range of the reference plane deviation within a sector.

5.2.5 *ROA (edge roll off amount)* — the displacement from the reference line at the measurement point in the near-edge region of an un-chucked silicon wafer. ROA is defined as positive in the direction away from the reference line.

5.2.6 *ZDD* — measure of near-edge curvature of a silicon wafer equal to the radial double derivative of the coordinate z perpendicular to the median plane of the wafer.

6 Summary of Practice

6.1 All partial sites are used for metric calculation. Partial sites are defined by FQA, the site size and offset. Required exclusions are defined.

6.2 A thickness data array is acquired.

6.3 The data array is used to construct a reference plane in each site.

6.4 PSFQR for each site is calculated as the range of the reference plane deviation within the site.

6.5 PSFQD for each site is calculated as the reference plane deviation within the site having the largest absolute value within the site while retaining the sign.

6.6 Recipe parameters are reported.