

SEMI M71-0120

SPECIFICATION FOR SILICON-ON-INSULATOR (SOI) WAFERS FOR CMOS LSI

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on August 19, 2019. Available at www.semiviews.org and www.semi.org in January 2020; originally published July 2007; previously published September 2012.

1 Purpose

1.1 This Specification defines thin-layer silicon-on-insulator (SOI) wafer requirements for CMOS large-scale integrated circuit (LSI) devices. In the case of 200 and 300 mm wafers this Specification is targeted for nodes from 130 to 14 nm. In the case of 150 mm wafers, older LSI generations are included as well. By defining parameters, inspection procedures and acceptance criteria, both suppliers and customers may uniformly define product characteristics and quality requirement.

2 Scope

2.1 This Specification covers SOI wafers manufactured by both SIMOX (Separation by **I**mplantation of **O**xxygen) or wafer bonding for layer transfer. It defines the properties of SOI wafers that are meant for use in LSI CMOS applications. It specifies the general characteristics of 200 and 300 mm notched SOI wafers. It facilitates selection of customer-driven parameters for 300 mm wafers with the Si film thickness from 8 to 300 nm, and for 200 mm wafers with the Si film thickness from 20 to 300 nm. Furthermore, this Specification also covers 150 mm wafers that typically have a flat instead of a notch. This Specification is intended to be used with the polished wafer specification (SEMI M1). In the case when epitaxial layers are used in fabrication of SOI wafers, the epitaxial wafer specification (SEMI M62), which defines the properties of the epitaxial layer, should also be utilized.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI 3D4 — Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks

SEMI 3D13 — Guide for Measuring Voids in Bonded Wafer Stacks

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M41 — Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

SEMI M62 — Specification for Silicon Epitaxial Wafers

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Test Method for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

3.2 *ANSI Standard*¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standard*²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specified Precision, the Average for a Characteristic of a Lot or Process

3.4 *ISO Standard*³

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence (TXRF) Spectroscopy

3.5 *JEITA Standards*⁴

JEITA EM-3501 — Standard Methods for Determining the Orientation of a Semiconductor Silicon Single Crystal

JEITA EM-3505 — Height Calibration in 1 nm Order for AFM

JEITA EM-3603B — Standard for SOI Wafers and Metrology

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 For general terminology for silicon wafers, including SOI wafers, and silicon technology, please refer to the SEMI Standards Compilation of Terms (COTs), a list of the current Abbreviations, Acronyms, Definitions, and Symbols. Previously, this was covered in SEMI M59.

5 Ordering Information

5.1 Purchase orders for SOI wafers furnished to this specification shall include the items indicated in 6-1 through 6-6 of Part 6 of the Specification Format for Order Entry (for SOI wafers) shown in Table 1. Other specified characteristics, as required, may be added in 6-7 of the format.

5.2 In addition, the purchase order shall include:

- the material in Part 1 (General Information) of the Specification Format for Order Entry, in SEMI M1,
- specifications for the substrate wafers of the appropriate characteristics as defined in Part 2 (Polished Wafer or Substrate) also in SEMI M1, and
- specifications for an epitaxial layer as defined in SEMI M62, as needed.

NOTE 1: Note that the orientation of single crystal is differently specified in SEMI MF26 and JEITA EM-3501.

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² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>

³ International Organization for Standardization, ISO Central Secretariat, BIBC II, Chemin de Blandonnet 8, CP 401, 1214 Vernier, Geneva, Switzerland; Telephone: +41.22.749.01.11, <http://www.iso.org>

⁴ Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; <http://www.jeita.or.jp>

Table 1 Silicon Wafer Specification Format for Order Entry, Part 6, SOI Wafers for CMOS LSI Applications

ITEM		SPECIFICATION	MEASUREMENT METHOD
6-1 SOI LAYER CHARACTERISTICS (Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify an SOI wafer.)			
♦	6-1.1	Type of SOI	☐ Bonded; ☐ SIMOX
	6-1.2	Starting silicon wafer for SOI	☐ Polished; ☐ Epitaxial ☐ Other: (specify) _____
♦	6-1.3	Surface Silicon Thickness	☐ nm ☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry; ☐ Other: (specify) _____
	6-1.4	Surface Silicon Thickness Mean Value Variation	Not greater than $\pm$ [] nm ☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry ☐ Other: (specify) _____
♦	6-1.5	Surface Silicon Thickness Variation in Wafer	Not greater than $\pm$ [] %; $\pm$ [] nm
♦	6-1.6	Crystal Orientation	(100) $\pm$ [] ° ☐ Other: (specify) _____ ☐ SEMI MF26 (X-ray); ☐ JEITA EM-3501; ☐ Other: (specify) _____
♦	6-1.7	Notch Orientation	<110> <100> ☐ Other: (specify) _____ Tolerance $\pm 1^\circ$ SEMI MF1152
	6-1.8	Rotation Misalignment, SOI layer to Base wafer	Not greater than $\pm$ [] ° for Bonded 200 mm and 300 mm diameter wafers. Not greater than $\pm$ [] ° for Bonded 150 mm wafers. ☐ Visual; ☐ Other: (specify) _____
	6-1.9	Edge Exclusion, Nominal, Determined from FQA (Fixed Quality Area) diameter	☐ mm
	6-1.10	Non-SOI Edge Area	Not greater than [] mm for Bonded ☐ Visual; ☐ Other: (specify) _____
	6-1.11	Conductivity Type	☐ p-type ☐ n-type ☐ SEMI MF42; ☐ Other: (specify) _____
	6-1.12	Dopant	☐ B ☐ P ☐ Other: (specify) _____ ☐ Secondary ion mass spectroscopy; ☐ Other: (specify) _____
	6-1.13	Resistivity (Center Point)	☐ Ohm cm ☐ 4-point probe [SEMI MF84]
	6-1.14	SOI Etch Pit	Not greater than [] cm ⁻² ☐ Secco Etching; ☐ Other: (specify) _____
	6-1.15	Threading Dislocation	Not greater than [] cm ⁻² ☐ Secco Etching; ☐ Other: (specify) _____
	6-1.16	HF Defect	Not greater than [] cm ⁻² ☐ HF Etching; ☐ Other: (specify) _____
	6-1.17	Surface Silicon Layer (SSL) Void or Void between bonded wafers	Not greater than [] ☐ SSIS; ☐ Visual; ☐ SEMI 3D13; ☐ Other: (specify) _____
	6-1.18	Front Si Surface Roughness	
	6-1.18.1	rms @ 2 μ m $\times$ 2 μ m	Not greater than [] nm ☐ JEITA EM-3505 (AFM); ☐ Other: (specify) _____

ITEM			SPECIFICATION	MEASUREMENT METHOD
	6-1.18.2	rms @ 10 $\mu\text{m} \times 10 \mu\text{m}$	Not greater than [] nm	☐ JEITA EM-3505 (AFM); ☐ Other: (specify) _____
	6-1.18.3	rms @ [] $\mu\text{m} \times [] \mu\text{m}$	Not greater than [] nm	☐ JEITA EM-3505 (AFM); ☐ Other: (specify) _____
	6-1.18.4	rms @ [] $\mu\text{m} \times [] \mu\text{m}$	Not greater than [] nm	☐ JEITA EM-3505 (AFM); ☐ Other: (specify) _____
	6-1.19	Front Surface Metal Contamination		
	6-1.19.1	Iron	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.19.2	Chromium	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.19.3	Nickel	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.19.4	Copper	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.20	Other Front Surface Metal Contamination (List Separately)		
	6-1.20.1	_____	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.20.2	_____	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.20.3	_____	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.20.4	_____	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.20.5	_____	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-1.20.6	_____	Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
6-2 BOX CHARACTERISTICS (Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify a silicon wafer.)				
♦	6-2.1	BOX Thickness	[] nm	☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry; ☐ Other: (specify) _____
♦	6-2.2	BOX Thickness Variation	Not greater than $\pm []\%$; $\pm []$ nm	☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry; ☐ Other: (specify) _____
	6-2.3	Bonded Interface Location for Bonded Wafers	☐ At SOI/BOX Interface; ☐ Within BOX Layer; ☐ At BOX/Substrate Interface	
	6-2.4	BOX Pinholes	Not greater than [] cm ⁻²	☐ Cu plating; ☐ BOX capacitor; ☐ Other: (specify) _____
	6-2.5	Dielectric Breakdown	Greater than [] MV/cm	☐ BOX capacitor; ☐ Other: (specify) _____
6.3 BASE WAFER CHARACTERISTICS (for Bonded SOI Only)				
♦	6-3.1	Crystal Orientation	(100) $\pm []^\circ$ ☐ Other: (specify) _____	☐ SEMI MF26 (X-ray); ☐ JEITA EM-3501; ☐ Other: (specify) _____
♦	6-3.2	Notch Orientation	<110> <100> ☐ Other: (specify) _____ Tolerance $\pm 1^\circ$	SEMI MF1152

ITEM		SPECIFICATION	MEASUREMENT METHOD
	6-3.3	Crystal Type	☐ Polished; ☐ Epitaxial ☐ Other: (specify) _____
◆	6-3.4	Conductivity Type	☐ p-type ☐ n-type ☐ SEMI MF42; ☐ Other: (specify) _____
◆	6-3.5	Dopant	☐ B ☐ P ☐ Other: (specify) _____
◆	6-3.6	Resistivity (Center Point)	☐ Ohm cm ☐ 4-point probe [SEMI MF84]
	6-3.7	Interstitial Oxygen	☐ ppm IR absorption (SEMI MF1188)
	6-3.8	Bulk Micro Defects	As agreed between supplier and customer IR absorption (SEMI MF1188)
6-4 DIMENSIONAL CHARACTERISTICS			
	6-4.1	Warp	Not greater than ☐ μm ☐ SEMI MF1390; ☐ SEMI 3D4; ☐ Other: (specify) _____
	6-4.2	Flatness, site	As agreed between supplier and customer
	6-4.3	Void (Non-Bond)	As agreed between supplier and customer ☐ SEMI 3D13 (specify) _____
6-5 FRONT SURFACE INSPECTION CHARACTERISTICS			
	6-5.1	Scratch	☐ None ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-5.2	Haze	☐ None ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-5.3	LLS	Size: $\geq$ ☐ μm (LSE) Count: $\leq$ ☐ ☐ per wafer; ☐ per cm ² ☐ SSIS; ☐ Other: (specify) _____
	6-5.4	Slip	As agreed between supplier and customer ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-5.5	Edge Chip	☐ SEMI M1, Table 10; ☐ Other: (specify) _____ ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-5.6	Edge Crack	☐ SEMI M1, Table 10; ☐ Other: (specify) _____ ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-5.7	Foreign Matter	As agreed between supplier and customer ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
6-6 BACK SURFACE CHARACTERISTICS			
	6-6.1	Scratch	☐ None ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-6.2	Boatmark	☐ None ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-6.3	Backside Oxide Thickness	☐ nm ☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry; ☐ Other: (specify) _____
	6-6.4	Back Surface Metal Contamination	
	6-6.4.1	Iron	Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-6.4.2	Chromium	Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
	6-6.4.3	Nickel	Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____

ITEM		SPECIFICATION	MEASUREMENT METHOD
6-6.4.4	Copper	Not greater than $[] \times 10^{[]}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
6-6.5	Other Back Surface Metal Contamination (List Separately)		
6-6.5.1	_____	Not greater than $[] \times 10^{[]}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
6-6.5.2	_____	Not greater than $[] \times 10^{[]}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
6-6.5.3	_____	Not greater than $[] \times 10^{[]}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
6-6.5.4	_____	Not greater than $[] \times 10^{[]}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
6-6.5.5	_____	Not greater than $[] \times 10^{[]}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____
6-6.5.6	_____	Not greater than $[] \times 10^{[]}$ atoms/cm ²	☐ ISO 14706 (TXRF); ☐ ICP-MS; ☐ AAS; ☐ Other: (specify) _____

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures.

5.3.2 Certification (if required).

5.3.3 Packing and marking requirements.

6 Requirements for Specifying SOI Wafers

6.1 It is essential to specify if the SOI wafers are built by SIMOX or wafer bonding for layer transfer technology. For bonded SOI, different crystal and orientational characteristics may be selected for the active SOI layer versus the base wafer, enabling an additional dimension for device design and functionality. Base wafer characteristics are listed in section 6.3 of Table 1. Base wafer characteristics apply to bonded SOI only. For SIMOX, SOI Layer Characteristics, section 6.1 of Table 1, define the characteristics of the both SOI and base wafer.

6.2 SOI wafers shall meet all requirements specified in the purchase order including those requirements related to the base wafer, the epitaxial layer (if needed), and the Si and buried oxide layer properties.

6.3 It is also essential to specify appropriate test methods in each case.

6.4 Related Information 1 provides a guide for specifying 200 and 300 mm SOI wafers for the 130 nm CMOS LSI technology generation and beyond, with the Si film thickness from 20 to 200 nm.

6.5 Related Information 2 provides a guide for specifying 150 nm SOI wafers for CMOS LSI.

6.6 Related Information 3 provides a guide for specifying 300 mm Extremely Thin SOI wafers (Si film 8 to 20 nm) that are primarily meant for fully depleted (FD) transistors at the 22 nm CMOS LSI technology generation and beyond.

7 Sampling Plan

7.1 Unless otherwise specified, ASTM E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQ Z1.4. Each quality characteristic shall be assigned with an acceptable quality level (AQL) of lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between users and suppliers.

8 Test Methods

8.1 Thickness of Surface Silicon Layer and Buried Oxide Layer

8.1.1 *Measurement Methods* — Two noncontact, nondestructive optical characterization techniques, spectroscopic ellipsometry (SE) and spectroscopic reflectometry, have proven useful both for surface silicon layer and buried oxide (BOX) layer thickness measurements. Both techniques use reflected light to allow deduction of the thickness and refractive index of thin layers. In both cases, layer thickness and index of refraction data must be ‘backed out’ of the measured optical data by a process of successive approximations. Silicon islands in the BOX layer of SIMOX and interface non-uniformity may reduce accuracy of the measurements.

8.1.1.1 *Spectroscopic Ellipsometry (SE) Measurement* — In this measurement, white light from a xenon arc lamp passes through a polarizing rotating filter and illuminates the sample site under study; reflected light passes through an analyzer to a monochromator and photomultiplier detector. For each wavelength, reflectivity oscillates with polarizer rotation; the magnitude and phase of reflectivity changes are measured to determine ellipsometric angles, δ and Ψ . The two measured spectra are fit by successive approximations to allow determination of the surface silicon layer and BOX layer thickness and oxide composition. For SE, the choice of instrument and associated model and fitting parameters affect the confidence-of-fit, so they should be taken into account in the user-supplier agreement.

8.1.1.2 *Spectroscopic Reflectometry Measurement* — In this measurement, light from a xenon arc lamp passes through a grating monochromator or optical band-pass filters and illuminates the sample site under study; reflected light is gathered by a detector. Specular reflectivity is plotted as a function of wavelength from 0.4 to 1.1 μm . The analysis proceeds by making successively better approximations to index of refraction and absorption of each layer until an acceptable fit is achieved.

8.1.1.3 *Optical Model Fitting and Correlation* — There are slight, systematic differences between layer thickness measured by SE and spectroscopic reflectometry. Because of this, users and suppliers should specify the actual measurement method to be used. The two methods offer results that are reproducible and well-correlated with each other over a wide range of conditions. If both measurement techniques are used, it is recommended that the reflectance system measurements be calibrated to fit the results of the SE.

8.1.2 *Measurement Positions* — The measurement strategy is to make a detailed measurement with an accurate fit on at least nine wafer sites, for example, the wafer center, four points at half of the wafer radius and four points at 10 mm from the wafer edge. The number and position of wafer sites to be monitored should be agreed on between users and suppliers. Generally, the greater the variability relative to the mean, the larger the number of sites that should be monitored. In each case, the measurement system supplies a ‘goodness-of-fit’ parameter that indicates a level of confidence in the fit to the measured data.

8.1.3 *Surface Silicon Layer and Buried Oxide (BOX) Layer Thickness* — Spectra for each site are fit independently with both the surface silicon and BOX layer thickness as adjustable parameters. Both the mean thickness and the uniformity should be specified.

8.1.4 Surface Silicon Thickness Mean Value Variation Wafer-to-Wafer

8.1.4.1 After surface silicon layer thickness is measured for predetermined number of wafers and mean value of surface silicon thickness is derived for each wafer, the maximum and the minimum values are chosen, and then the variation (nm) is calculated as $\pm(1/2)(\text{Maximum mean value} - \text{Minimum mean value})$.

8.1.4.2 In case of quite large number of wafers (e.g., a few hundred), the variation (nm) can be calculated as $\pm 3\sigma$ (3 times the standard deviation) under agreement between suppliers and customers.

8.1.5 Surface Silicon Thickness Variation Within Wafer

8.1.5.1 After surface silicon layer thickness is measured at predetermined number of points within an SOI wafer, the maximum and the minimum values are chosen, and then the variation (nm) is calculated as $\pm(1/2)(\text{Maximum value} - \text{Minimum value})$.

8.1.5.2 In case of multipoint measurements (e.g., a few hundred) within an SOI wafer, the variation (nm) can be calculated as $\pm 3\sigma$ (3 times the standard deviation) under agreement between supplier and customer.

8.1.6 Buried Oxide (BOX) Relative (in %) Thickness Variation

8.1.6.1 After BOX thickness is measured for predetermined number of points on predetermined number of wafers, the maximum and the minimum values are chosen, and then the variation (%) is calculated as $\pm[(\text{Maximum value} - \text{Minimum value}) \times 100]/(2 \times \text{mean value})$.

8.1.6.2 In case of multipoint measurements (e.g., a few hundred) within an SOI wafer or quite large number of wafers (e.g., a few hundred), the variation (%) can be calculated as $\pm 300\sigma/(\text{mean value})$ under agreement between supplier and customer.

8.1.6.3 The thickness of BOX measured after removal of the silicon film above it is frequently slightly different (± 2 nm) than the thickness in a Si/BOX stack. This is not caused by a physical change in the oxide film during the removal of silicon, and the exposed BOX may appear thicker or thinner than in its Si-covered configuration. Because of these discrepancies, the measurement configuration should always be specified.

8.2 Dopant Concentration

8.2.1 Secondary ion mass spectroscopy (SIMS) is utilized to determine dopant concentration in surface silicon layer.

8.2.2 The acceptable dopant concentrations are to be determined by agreement between supplier and customer.

8.3 Defects in Surface Silicon Layer (SSL)

8.3.1 *SOI Etch Pits* — Defects in surface silicon layer including stacking faults, threading dislocations and other crystal defects are evaluated by destructive chemical etching and microscopic etch pit density measurements. The appropriate evaluation procedure for SOI wafers, which depends on type of defects targeted and thickness of surface silicon layers, is determined by agreement between users and suppliers. More detailed analysis of SOI etch pits is provided in JEITA EM-3603B.

8.3.2 *Environmentally Friendly Etchants for Pits* — Because of environmental concerns, it is recommended—particularly if etching is used routinely on significant quantities of samples—that a chromium-free etchant, as described in JEITA EM-3603B or SEMI MF1809 be used.

8.3.3 *HF Defects* — Measurement of the microscopic etch pit density following an HF etch is commonly used to disclose defects in SOI material. Pitting of surface silicon may be present before the HF etch or be caused by HF etching. For this destructive measurement, a whole wafer or at least one quarter of a wafer should be used. The sample is placed in concentrated (49%) HF for 10 to 15 minutes or diluted (e.g., 25%) HF for longer time (e.g., 3 to 4 hours), then removed, rinsed and dried. If there are pits or voids and/or metal particles or silicides formed in the surface silicon layer, the HF etches the metals/silicides and then etches the buried oxide. This results in local etching of BOX with 25 to 50 μm diameter (depending on the HF concentration and the etch time) centered on the original defects. The defect density is then measured in an optical microscope using a 5 $\times$ objective and 10 $\times$ eyepiece or comparable setup. The samples should be scanned for whole surface within edge exclusion boundary.

8.3.4 SSL Voids

8.3.4.1 Voids are determined as an unbonded area on bonded SOI wafers (see SEMI M41). Because the SOI layers in thin bonded SOI wafers are typically 0.2 μm thick or thinner, void areas are broken and SOI layers as well as BOX are usually absent. By this reason, SSL voids are specified as local absence of SOI layers and/or BOX in bonded wafers in this specification.

8.3.4.2 *Visual Inspection* — Under visible light, the edge of SSL voids is detected because the edge area is step-shaped due to absence of SOI layers and/or BOX layers. See ¶ 8.8 for inspection conditions.

8.3.4.3 *Detection as Large LLS* — The edge of local absence of SOI layer and/or BOX scatters light. Therefore, SSL voids are detected as large LLS. See ¶ 8.7.2 for the principle. A size of LLS corresponding to various sizes of SSL voids should be calibrated or correlated by comparison of defects one by one using a microscope.

8.4 Surface Roughness

8.4.1 *Atomic Force Microscope (AFM)* — By contacting the probe equipped with the cantilever onto the wafer surface of the sample, and by scanning the cantilever and detecting the variation by optical method, the roughness information is obtained. A tapping mode is commonly used.