

SEMI M71-0707

SPECIFICATION FOR SILICON-ON-INSULATOR (SOI) WAFERS FOR CMOS LSI 130 nm TECHNOLOGY GENERATION AND BEYOND

This standard was technically approved by the global Silicon Wafer Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on April 25, 2007. It was available at www.semi.org in June 2007 and on CD-ROM in July 2007.

1 Purpose

1.1 This specification defines thin-layer silicon-on-insulator (SOI) wafer requirements for CMOS large-scale integrated circuit (LSI) devices for the 130 nm technology node and beyond (65 nm, 45 nm, etc). By defining parameters, inspection procedures and acceptance criteria, both users and suppliers may uniformly define product characteristics and quality requirement.

2 Scope

2.1 This specification defines the properties of SOI wafers that are meant for use in LSI CMOS applications. It specifies the general characteristics of 200 mm and 300 mm SOI wafers and it facilitates selection of customer-driven parameters for ultrathin SOI (Si film 20–50 nm). It also includes specifications for 200 and 300 mm diameter SOI wafers that have somewhat thicker Si films (50 nm < Si < 200 nm) that are currently covered in SEMI M47. This specification is intended to be used with the polished wafer specification [SEMI M1]. In the case when epitaxial layers are used in fabrication of SOI wafers, the epitaxial wafer specification [SEMI M62], which defines the properties of the epitaxial layer, should also be utilized.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards

- SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers
- SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers
- SEMI M20 — Practice for Establishing a Wafer Coordinate System
- SEMI M47 — Specification for Silicon-on-insulator (SOI) Wafers for CMOS LSI Applications
- SEMI M59 — Terminology for Silicon Technology
- SEMI M62 — Specification for Silicon Epitaxial Wafers
- SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal
- SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces
- SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

3.2 ANSI Standard¹

- ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

¹ American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023; <http://www.ansi.org>

3.3 ASTM Standard²

E 122 — Practice for Calculating Sample Size to Estimate, with a Specified Tolerable Error, the Average for a Characteristic of a Lot or Process

3.4 JEITA Standards³

EM-3501 — Standard methods for determining the orientation of a semiconductor silicon single crystal

EM-3603B — Standard for SOI wafers and metrology

NOTICE: As listed or revised, all documents cited shall be the latest publications of adopted standards.

4 Terminology

4.1 General terminology for silicon wafers and silicon technology is covered in SEMI M59.

4.2 Terms related to SOI wafers are as follows:

4.2.1 *base silicon substrate* — the wafer used as a support for the multilayer structure of oxide and silicon that comprises an SOI wafer. In the case of SIMOX technology, it is the starting wafer into which the oxygen is implanted. Also known as *handle wafer*.

4.2.2 *BOX* — buried oxide layer.

4.2.3 *bonded SOI wafer* — an SOI wafer made by bonding two silicon wafers with an insulating layer that is typically thermally grown silicon dioxide between them.

4.2.4 *SIMOX wafer* — SOI wafer made by implanting oxygen into a base silicon substrate.

4.2.5 *SOI layer* — the single crystalline (monocrystalline) silicon film that is separated by an insulating layer, typically but not necessarily silicon dioxide (SiO₂), from a base silicon substrate. Note that polycrystalline or amorphous silicon films on oxidized silicon wafers are not considered to be SOI layers. Also called *top silicon film*.

5 Ordering Information

5.1 Purchase orders for SOI wafers furnished to this specification shall include the items indicated in §§ 6-1 through 6-5 of Part 6 of the Specification Format for Order Entry (for SOI wafers) shown in Table 1 (Appendix 2 in SEMI M18). Other specified characteristics, as required, may be added in § 6-6 of the format.

5.2 In addition, the purchase order shall include:

- the material in Part 1 (General Information) of the Specification Format for Order Entry, in SEMI M1,
- specifications for the substrate wafer of the appropriate characteristics as defined in Part 2 (Polished Wafer or Substrate) also in SEMI M1, and
- specifications for the epitaxial layer as defined in SEMI M62, as needed.

NOTE 1: Note that the orientation of single crystal is differently specified in SEMI MF26 and JEITA EM-3501.

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures.

5.3.2 Certification (if required).

5.3.3 Packing and marking requirements.

² Available from ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA. Telephone: 610.832.958; Fax: 610.832-9555; <http://www.astm.org>. ASTM E 122 is published in Volume 14.02 of *Annual Book of ASTM Standards* while ASTM E 673 is published in Volume 3.06.

³ Japan Electronics and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan. Tel: 81.3.3518.6434; Fax: 81.3.3295.8727; <http://www.jeita.or.jp>

Table 1 Silicon Wafer Specification Format for Order Entry, Part 6, SOI Wafers for CMOS LSI Applications

ITEM		SPECIFICATION	MEASUREMENT METHOD
6-1. SOI LAYER CHARACTERISTICS (Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify an SOI wafer.)			
♦ 6-1.1	Type of SOI	☐ Bonded; ☐ SIMOX	
6-1.2	Starting silicon wafer for SOI	☐ Polished; ☐ Epitaxial ☐ Other: (specify) _____	
♦ 6-1.3	Surface Silicon Thickness	☐ (nm)	☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry; ☐ Other: (specify) _____
6-1.4	Surface Silicon Thickness Mean Value Variation	Not greater than $\pm$ [] nm	☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry ☐ Other: (specify) _____
♦ 6-1.5	Surface Silicon Thickness Variation in Wafer	Not greater than $\pm$ [] %; $\pm$ [] nm	
6-1.6	Crystal Orientation	(100) $\pm$ [] °	☐ SEMI MF26 (X-Ray); ☐ Other: (specify) _____
6-1.7	Rotation Misalignment	Not greater than [] mm for Bonded	☐ Visual; ☐ Other: (specify) _____
6-1.8	Edge Exclusion, Nominal, Determined from FQA (Fixed Quality Area) diameter	[] mm	
6-1.9	Non-SOI Edge Area	Not greater than [] mm for Bonded	☐ Visual; ☐ Other: (specify) _____
6-1.10	Conductivity Type	☐ p-type ☐ n-type	☐ SEMI MF42; ☐ Other: (specify) _____
6-1.11	Dopant	☐ B ☐ P ☐ Other: (specify) _____	☐ Secondary ion mass spectroscopy; ☐ Other: (specify) _____
6-1.12	Dopant Concentration	[] (atoms/cm ³)	☐ Secondary ion mass spectroscopy; ☐ Other: (specify) _____
6-1.13	SOI Etch Pit	Not greater than [] cm ⁻²	☐ Secco Etching; ☐ Other: (specify) _____
6-1.14	Threading Dislocation	Not greater than [] cm ⁻²	☐ Secco Etching; ☐ Other: (specify) _____
6-1.15	HF Defect	Not greater than [] cm ⁻²	☐ HF Etching; ☐ Other: (specify) _____
6-1.16	Void	Not greater than []	☐ SSIS; ☐ Visual; ☐ Other: (specify) _____
6-1.17	Front Si Surface Roughness		
6-1.17.1	rms @ 2 μ m $\times$ 2 μ m	Not greater than [] nm	☐ JIS EM-3503 (AFM); ☐ Other: (specify) _____
6-1.17.2	rms @ 10 μ m $\times$ 10 μ m	Not greater than [] nm	☐ JIS EM-3503 (AFM); ☐ Other: (specify) _____
6-1.17.3	rms @ [] μ m $\times$ [] μ m	Not greater than [] nm	☐ JIS EM-3503 (AFM); ☐ Other: (specify) _____
6-1.17.4	rms @ [] μ m $\times$ [] μ m	Not greater than [] nm	☐ JIS EM-3503 (AFM); ☐ Other: (specify) _____
6-1.18	Front Surface Metal Contamination		
6-1.18.1	Iron	☐ Not greater than [] $\times 10^{11}$ atoms/cm ²	☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____

ITEM		SPECIFICATION	MEASUREMENT METHOD
	6-1.18.2	Chromium	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.18.3	Nickel	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.18.4	Copper	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.19	Other Front Surface Metal Contamination (List Separately)	
	6-1.19.1	_____	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.19.2	_____	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.19.3	_____	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.19.4	_____	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.19.5	_____	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
	6-1.19.6	_____	☐ Not greater than ☐ $\times 10^{11}$ atoms/cm ² ☐ ICP/MS; ☐ AAS; ☐ SEMI M33 (TXRF); ☐ ISO 14706 (TXRF); ☐ Other: (specify) _____
6-2. BOX CHARACTERISTICS (Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify a silicon wafer.)			
♦	6-2.1	BOX Thickness	☐ nm ☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry; ☐ Other: (specify) _____
♦	6-2.2	BOX Thickness Variation	Not greater than $\pm$ ☐ %; $\pm$ ☐ nm ☐ Spectroscopic ellipsometry; ☐ Spectroscopic reflectometry; ☐ Other: (specify) _____
	6-2.3	Bonded Interface Location for Bonded Wafers	☐ At SOI/BOX Interface; ☐ Within BOX Layer; ☐ At BOX/Substrate Interface
	6-2.4	BOX Pinholes	Not greater than ☐ cm ⁻² ☐ Cu plating; ☐ BOX capacitor; ☐ Other: (specify) _____
	6-2.5	Dielectric Breakdown	Greater than ☐ MV/cm ☐ BOX capacitor; ☐ Other: (specify) _____
6-3. DIMENSIONAL CHARACTERISTICS			
	6-3.1	Warp	Not greater than ☐ μ m ☐ SEMI MF1390; ☐ Other: (specify) _____
	6-3.2	Flatness, site	See #1
6-4. FRONT SURFACE INSPECTION CHARACTERISTICS			
	6-4.1	Scratch	☐ None ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____
	6-4.2	Haze	☐ None ☐ SEMI MF523 (Visual); ☐ Other: (specify) _____