

SEMI M74-1108 (Reapproved 1018) SPECIFICATION FOR 450 mm DIAMETER MECHANICAL HANDLING POLISHED WAFERS

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on August 17, 2018. Available at www.semiviews.org and www.semi.org in October 2018; originally published November 2008; previously published April 2013.

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1 Purpose

1.1 This Standard specifies 450 mm diameter mechanical handling wafers intended for use in research, development and early design investigation of 450 mm semiconductor equipment such as 450 mm wafers, carriers, load ports, AMHS, and robotics.

2 Scope

2.1 This Specification covers dimensional requirements for 450 mm diameter polished silicon wafers. This Specification is intended to address a short-term need for handling wafers. It is not intended to specify wafers used in process development or for technology-specific circuit-quality applications. This Standard should be superseded by a process development wafer specification, a prime wafer specification and technology-specific guidelines for circuit-quality wafers.

2.2 A complete purchase specification may require that additional physical properties be specified along with test methods for determining their magnitude (refer to § 5).

2.3 Wafers meeting the basic specification requirements herein are suitable for use as ‘mechanical handling’ wafers for equipment set-up and robotic handling applications.

2.4 For reference purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Non-Contact Scanning

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI® Standards*¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM® Standards*²

ASTM E122 — Standard Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

3.4 *DIN Standards*³

DIN 50441-1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

DIN 50441-2 — Determination of the Geometric Dimensions of Semiconductor Slices: Testing of Edge Rounding

3.5 *JSA Standards*⁴

JIS H 0611 — Methods of Measurement of Thickness, Taper and Bow for Silicon Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many of the terms used in this Specification are defined in SEMI M59.

5 Wafer Ordering Information

5.1 Purchase orders for silicon wafers furnished to this Specification shall include the following items:

5.1.1 Wafer type: polycrystalline-sintered or single crystal (monocrystalline). Lot acceptance procedures (§ 7).

5.1.2 Test methods for specified attributes (§ 8).

5.1.3 Certification (if required) (§ 9).

5.1.4 Packing and Package Labeling (§ 10).

5.2 *Optional Criteria* — The following items may also be specified in addition to those listed above if they are considered to be necessary for the application for which the wafers are to be employed.

5.2.1 Optional wafer identification mark symbol or symbols, if any (refer to § 6.3.2).

5.3 *Additional Criteria* — Any additional criteria considered to be necessary for the application for which the wafers are to be employed may also be specified, as agreed between supplier and customer.

6 Requirements

6.1 *Material* — Wafers shall consist of silicon, either polycrystalline-sintered or single crystal (monocrystalline).

6.2 *Dimensions and Permissible Variations* — Wafers shall conform to the dimensions and dimensional tolerances as specified for the attributes listed in Table 1.

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² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

³ Deutsches Institut für Normung e.V., Am DIN-Platz, Burggrafenstrasse, D-10787 Berlin, Germany; Telephone: +49.30.2601.0, Fax: +49.30.2601.1231, <http://www.din.de>.

⁴ JSA Group, Mita MT Bldg., 3-13-12 Mita, Minato-ku, Tokyo, 108-0073, Japan; Telephone: +81.50.1741.7520, Fax: +81.3.4231.8650, <http://www.jsa.or.jp>.

Table 1 Dimensional Requirements

<i>Property</i>	<i>Specification</i>
DIAMETER	450.0 ± 0.2 mm
THICKNESS, CENTER POINT	925 ± 25 µm
NINE-POINT THICKNESS VARIATION, less than	10 µm
NOTCH DIMENSIONS (refer to Figure 1) Depth Angle	1.00 mm + 0.25 mm – 0.00 mm 90° + 5° – 1°
FRONT SURFACE	POLISHED
BACK SURFACE FINISH (GLOSS)	POLISHED
EDGE PROFILE SURFACE FINISH	POLISHED

#1 Since diameter tolerance statistics are not available for 450 mm Mechanical Wafer Manufacturing at this time, ±0.2 mm wafer diameter tolerance is used as a starting point specification based on existing 300 mm capability. However, some wafer handling robot design may need ±0.1 mm diameter tolerance for throughput needs during development and prototyping evaluation. The wafer diameter tolerance specification will be revisited by the end of 2008 for a tighter specification, i.e., ±0.1 mm, when more silicon wafer manufacturer actual data is available.

#2 Shape is not specified. A reasonable target value for warp is considered to be <100 µm. The target warp value is expected to be adequate for many handling purposes. Processing may induce additional warp.

6.2.1 Fiducial Mark — A notch in conformance with the dimensions and tolerances of Figure 1 shall be placed on the periphery of the wafer.

6.2.1.1 For monocrystalline wafers the notch shall be placed at the end of a diameter corresponding to a <110> crystal direction within ±1°. This diameter is called the orientation fiducial axis. For (100) wafers, the allowable equivalent <110> directions are $[01\bar{1}]$, $[011]$, $[0\bar{1}1]$, and $[011]$.

6.2.1.2 For polycrystalline-sintered wafers the notch shall be placed at an arbitrary position on the periphery of the wafer.

6.2.2 Back Surface Finish — The back surface shall be polished.

6.2.3 Edge Profile and Edge Finish — The edge profile shall conform to the following requirements at all points on the wafer periphery (except interior portions of notches which are to be finished in accordance with the provisions of the purchase order or contract).

6.2.3.1 Edge Profile — When the wafer is aligned with the SEMI Wafer Edge Profile Template (refer to Figure 2 and Table 2) so that the *x*-axis of the template is coincident with the wafer surface and the *y*-axis of the template is tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template. (Refer to Figure 3 for examples of acceptable and unacceptable contours.) No sharp corners, points, or protrusions are permitted anywhere on the wafer edge contour.

6.2.3.2 Edge Profile Surface Finish — The edge profile surface finish is specified to be ‘polished,’ which is meant to imply a surface condition and not a particular processing technique.