

SEMI M76-0710

SPECIFICATION FOR DEVELOPMENTAL 450 mm DIAMETER POLISHED SINGLE CRYSTAL SILICON WAFERS

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on April 30, 2010. Available at www.semi.org in July 2010.

NOTICE: This Standard or Safety Guideline has an Inactive Status because the conditions to maintain Current Status have not been met. Inactive Standards or Safety Guidelines are available from SEMI and continue to be valid for use.

1 Purpose

1.1 The developmental wafers covered by this Specification are intended for use in research and development of process and metrology equipment and fabrication processes required for manufacturing high-density integrated circuits on 450 mm diameter single crystal silicon wafers. They can also be used to establish the techniques and metrology necessary to support a dimensional specification for 450 mm diameter circuit-quality (prime) wafers.

2 Scope

2.1 This Specification covers dimensional and crystallographic orientation requirements for 450 mm diameter, polished single crystal silicon wafers needed in development. This Document should be superseded by dimensional specification and technology-specific guidelines for circuit-quality wafers.

2.2 A complete purchase specification requires that additional physical properties be specified along with test methods for determining their magnitude. If a test instrument is not available, the acceptance criteria should be agreed upon between supplier and customer.

2.3 This Specification also contains guidance to assist equipment manufacturers and others to specify wafers for use in developing selected process equipment and unit processes.

2.4 The specification for 450 mm diameter mechanical handling wafers used in development of 450 mm semiconductor equipment such as 450 mm wafers carriers, load ports, Automated Materials Handling System (AMHS), and robotics has already been published as SEMI M74.

2.5 This Specification is not intended to be a product wafer specification.

2.6 For reference purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI E45 — Test Method for the Determination of Inorganic Contamination from Mini Environments Using Vapor Phase Decomposition-Total Reflection X-Ray Spectroscopy (VPD/TXRF), VPD-Atomic Absorption Spectroscopy (VPD/AAS), or Inductively Coupled Plasma-Mass Spectroscopy (VPD/ICP-MS)

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M59 — Terminology for Silicon Technology

SEMI M67 — Practice for Determining Wafer Near-Edge Geometry from a Measured Thickness Data Array Using the ESFQR, ESFQD and ESBIR Metrics

SEMI M68 — Practice for Determining Wafer Near-Edge Geometry from a Measured Height Data Array Using a Curvature Metric, ZDD

SEMI M70 — Practice for Determining Wafer-Near-Edge Geometry Using Partial Wafer Site Flatness

SEMI M73 — Test method for Extracting Relevant Characteristics from Measured Wafers Edge Profiles

SEMI M74 — Specification for 450 mm Diameter Mechanical Handling Polished Wafers

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Test Method for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1389 — Test Method for Photoluminescence Analysis of Single Crystal Silicon for III-V Impurities

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with *p*-Polarized Radiation Incident at the Brewster Angle

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 ANSI Standard¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: 212.642.4900, Fax: 212.398.0023, <http://www.ansi.org>

3.3 ASTM Standard²

ASTM E122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

3.4 ISO Standard³

ISO 17331 — Surface Chemical Analysis – Chemical Methods for Collection of Elements from the Surface of Silicon-Wafer Working Reference Materials and Their Determination by Total-Reflection X-Ray Fluorescence (TXRF) Spectroscopy

4 Terminology

4.1 Terms and acronyms associated with silicon wafers and silicon technology are listed and defined in SEMI M59.

5 Wafer Ordering Information

5.1 Purchase orders for silicon wafers furnished to this specification shall include the following items. Values for these items are given in Tables 1 and 2.

5.1.1 Developmental wafer monitor category.

5.1.2 Crystal Growth Method (see ¶ 6.3).

5.1.3 Conductivity Type and Dopant.

5.1.4 Resistivity or Resistivity Range.

5.1.5 Wafer edge profile type requested (see ¶ 6.4.7).

5.1.6 Lot Acceptance Procedures (see § 7).

5.1.7 Test methods for specified attributes (see § 8).

5.1.8 Certification (if required) (see § 9).

5.1.9 Packing and Package Labeling (see § 10).

5.2 *Optional Criteria* — The following items may also be specified in addition to those listed above if they are considered to be necessary for the application for which the wafers are to be employed (see Table 1).

5.2.1 Wafer identification mark symbol or symbols.

5.2.2 Wafer dimensional characteristics requirements; as specified in Appendix 1 of SEMI M1.

5.2.3 Particulate contamination (localized light scatterer) requirements (see ¶ 6.5.2).

5.2.4 Surface defect requirements, including surface metal contamination (see ¶ 6.5.3).

5.3 *Additional Criteria* — Any additional criteria considered to be necessary for the application for which the wafers are to be employed may also be specified, as agreed between supplier and customer (see Table 1).

6 Requirements

6.1 Table 1 and Table 2 contain detailed specifications for 450 mm diameter wafers intended for use in development. The requirements are organized by wafer categories and edge profile specification method. Table 1 details wafer required properties by category to assist manufacturers in choosing the most cost effective wafers for a given application. Table 2 details the different methods for specifying the edge profile requirements.

6.2 Wafer Categories

6.2.1 *Particle Monitors* — Wafers intended for use in evaluating the particulate contamination added by a process tool must have controlled front and back surface defect properties. Consequently, specifications are provided for front

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: 610.832.9585, Fax: 610.832.9555, <http://www.astm.org>

³ International Organization for Standardization, ISO Central Secretariat, 1, ch. de la Voie-Creuse, CP 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, <http://www.iso.org>

surface localized light scatterers (LLSs), edge chips, and scratches on both surfaces. If desired, a specification for back surface LLSs can be negotiated between supplier and purchaser.

6.2.2 Lithography Monitors — For development of lithographic and patterning equipment and processes, both surface flatness and surface defects must be carefully controlled.

6.2.3 Other Monitors — This column repeats the basic requirements for developmental wafers. Wafers in this category are not intended for use in particle counting or lithography and patterning. These wafers are suitable for use in process and inspection equipment development. When used for furnace and thermal processes development wafer back side, edge surface finish and oxygen content are critical issues in connection with the introduction of slip during high temperature processing. Bulk iron, oxidation induced stacking faults, and bulk microdefects all can influence wafer performance in thermal processing and should be controlled for critical tests; appropriate specification levels should be negotiated between supplier and purchaser.

Table 1 General Specification for Developmental 450 mm Diameter Polished Single Crystal Silicon Wafers

Item ^{#1}		Wafer Category			Measurement Method
		Particle Monitors	Lithography Monitors	Other Monitors	
2-1 GENERAL CHARACTERISTICS					
2-1.1	Growth Method	Cz or MCz			
2-1.3	Crystal Orientation	(100)			SEMI MF26 (x-ray)
2-1.4	Conductivity Type	p		p or n	SEMI M1, SEMI MF42
2-1.5	Dopant	B		B or P	SEMI M1, SEMI MF1389
2-1.6	FQA radius ^{#2}	223 mm			
2-1.8	Wafer surface declination in respect to crystal orientation	On-orientation 0.00° ± 1.00°			SEMI MF26 (x-ray)
2-2 ELECTRICAL CHARACTERISTICS					
2-2.1	Resistivity ^{#3} p-type wafers	0.005–100 Ω·cm	0.5–100 Ω·cm		SEMI M1, SEMI MF673
	n-type wafers	Not specified		1–20 Ω·cm	SEMI M1, SEMI MF673
2-2.2	Radial Resistivity Variation (RRG) ^{#4}	<10%			SEMI M1, SEMI MF81
2-3 CHEMICAL CHARACTERISTICS					
2-3.1	Oxygen Concentration	Not specified		Customer Specified	SEMI M1, SEMI MF1188, SEMI MF1366
2-3.2	Radial Oxygen Variation ^{#5}	Not specified		≤10%	SEMI MF951
2-4 STRUCTURAL CHARACTERISTICS					
2-4.1	Dislocation Etch Pit Density	≤10/cm ²			SEMI M1, SEMI MF1809
2-4.2	Slip	None			SEMI MF1809
2-4.4	Twin Boundary	None			SEMI MF1809
24.5	Swirl	None			SEMI MF1809
2-5 WAFER PREPARATION CHARACTERISTICS					
2-5.1	Wafer ID Marking ^{#6}	SEMI T7			SEMI T7
2-5.7	Edge surface conditions	Polished ^{#7}			
2-5.8	Back surface condition	Polished ^{#7}			