SEMI M79-0218
SPECIFICATION FOR ROUND 100 mm POLISHED MONOCRYSTALLINE GERMANIUM WAFERS FOR SOLAR CELL APPLICATIONS

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1 Purpose

1.1 These specifications cover substrate requirements for round 100 mm monocrystalline high-purity germanium wafers used in semiconductor and electronic device manufacturing.

2 Scope

2.1 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

2.2 These specifications are directed specifically to germanium wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.3 The material is single crystal germanium (Ge) with the following properties:

Table 1 Basic Properties of Single Crystal Ge

Property	*Value*
Lattice Parameter	5.658 Å
Crystal Structure	Diamond
Density	5.3234 g/cm^3
Melting Point	937°C
Dielectric Constant	16.2
Energy Gap	0.661 eV
Thermal Conductivity	0.58 W/cm/°C

2.4 For referee purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the non-s to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF43 — Test Method for Resistivity of Semiconductor Materials

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

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SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning (Withdrawn 0914)

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon and Wafers by X-Ray Techniques

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T5 — Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers

3.2 *ANSI Standard*[1]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standards*[2]

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, with Specified Precision, the Average for a Characteristic of a Lot or Process

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

3.4 *DIN Standards*[3]

DIN 50441-1 — Measurement of the Geometric Dimensions of Semiconductor Wafers: Thickness and Thickness Variation

DIN 50448 — Testing of Materials for Semiconductor Technology – Contactless Determination of the Electrical Resistivity of Semi-insulating Semiconductor Slices Using a Capacitive Probe

3.5 *JIS Standard*[4]

JIS H 0611 — Methods of Measurement of Thickness Taper and Bow for Silicon Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M1, the SEMI International Standards Compilation of Terms, and ASTM F154.

4.1 *Definitions*

4.1.1 *bow* — of a semiconductor wafer, a measure of concave or convex deformation of the median surface of a wafer, independent of any thickness variation which may be present. Bow is a bulk property of the test specimen, not a

[1] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, http://www.ansi.org

[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, http://www.astm.org

[3] Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany; http://www.din.de

[4] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: +81.3.3583.8005, Fax: +81.3.3586.2014, http://www.jsa.or.jp

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property of an exposed surface. Generally, bow is determined with a test specimen in a free, unclamped condition. Units of bow are generally micrometers.

4.1.2 *crystallite* — any part of the wafer, having an arbitrary orientation of its crystallographic axis in respect to the monocrystalline part of the wafer.

4.1.3 *dopant* — a chemical element, usually from the third or fifth column of the periodic table for the case of IV-IV compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.4 *edge contouring* — on wafers whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the wafer joining the front and back sides.

4.1.5 *edge exclusion* — the width X of a narrow band of wafer surface, located just inside the wafer edge, over which the values of the specified parameter do not apply. See definition of *fixed quality area* in Figure 1.

4.1.6 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal *edge exclusion*, *X*, over which the specified values of a parameter apply.

4.1.6.1 *Discussion* — The boundary of the FQA is at all points the distance *X* away from the periphery of a wafer of nominal dimensions (see Figure 1). The size of the FQA is independent of wafer diameter and flat length tolerances.

4.1.7 *lot* — for the purpose of this Document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.8 *surface orientation* — for example, (100), (111), etc. with a specified tilt angle and direction, for example, 2^0 towards a specific plane family, for example, <111>. Tolerance of the tilt, for example, $\pm 0.5^0$, should also be specified.

4.1.9 *total indicator reading (TIR)* — the smallest perpendicular distance between two planes, both parallel with the reference plane, which encloses all points on the front surface of a wafer within the FQA, the site, or the subsite, depending on which is specified.

4.1.10 *total thickness variation (TTV)* — the difference between the maximum and minimum thickness values of a wafer encountered during a scan pattern or a series of point requirements. TTV is generally expressed in micrometers.

4.1.11 *warp* — of a semiconductor slice or wafer, the difference between the maximum and minimum distance of the median surface of the wafer from a reference plane, encountered during a scan pattern. Warp is a bulk property of the test specimen, not a property of an exposed surface. Warp is generally expressed in micrometers.

5 Ordering Information

5.1 Examples of parameters described in ¶¶ 5.2.1 to 5.2.13 (below) are shown in Table 2. Additional information on items 5.2.14, 5.2.15 and 5.2.16 are described §§ 7, 10, and 11 (below).

5.2 Purchase orders for germanium wafers furnished to this Specification shall include the following items:

5.2.1 Nominal diameter,

5.2.2 Thickness,

5.2.3 Dopant,

5.2.4 Resistivity,

5.2.5 Total thickness variation (TTV),

5.2.6 Bow,

5.2.7 Warp,

5.2.8 Surface orientation,

5.2.9 Orientation flats,

5.2.10 Dislocation density or etch pit density (EPD),

5.2.11 Edge exclusion,

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