

SEMI M8-0301

SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON TEST WAFERS

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1 Purpose

1.1 This Specification covers requirements for virgin silicon test wafers to be used for testing and process monitoring in semiconductor manufacturing.

2 Scope

2.1 Dimensional and crystallographic orientation characteristics and limits on surface defects are the only standardized properties included in this Specification.

2.2 A complete purchase specification requires that additional physical properties be defined. These properties are listed, together with test methods suitable for determining their magnitude.

2.3 This Specification is directed specifically to silicon wafers with one polished surface. Wafers polished on both sides, or unpolished, or with epitaxial deposits are not covered; however, purchasers of such wafers may find this Specification to be a useful guide in defining their requirements.

2.4 This Specification classifies test wafers according to surface condition defect levels and dimensional tolerances. Test wafer classifications are summarized in Tables 1 and 2.

2.5 For applications placing higher demands on silicon wafers such as particle counting, measuring particle resolution in a photolithography process, or surface ion contamination monitoring, the user may reference the SEMI M1 or SEMI M24 Standards.

2.6 For referee purposes, U.S. customary units shall be used for wafers of 2- and 3-inch nominal diameter and SI (System International), commonly called metric units, for 100 mm and larger diameter wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M25 — Specification for Silicon Wafers for Calibration of Light Point Defect Wafer Inspection Systems with Respect to the Diameter of Polystyrene Latex Spheres

3.2 ANSI/ASQC Standards¹

For a comprehensive list of applicable ANSI/ASQC Standards, see those listed in Table 1 of SEMI M18.

3.3 ASTM Standards²

For a comprehensive list of applicable ASTM Standards, see those listed in Table 1 of SEMI M18.

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, <http://www.ansi.org>

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>

3.4 DIN Standards³

For a comprehensive list of applicable DIN Standards, see those listed in Table 1 of SEMI M18.

3.5 JIS Standards⁴

For a comprehensive list of applicable JIS Standards, see those listed in Table 1 of SEMI M18.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions of terms related to silicon wafer technology are given in ASTM Terminology F 1241.

4.2 Definitions for some additional terms are given in SEMI M1.

4.3 The following definitions apply in the context of this Specification:

4.3.1 *mechanical test wafer* — silicon wafer suitable for testing equipment with emphasis on dimensional and structural characteristics only.

4.3.2 *process test wafer* — silicon wafer suitable for processes as well as area and process cleanliness (higher grade than mechanical test).

4.3.3 *test wafer* — silicon wafer suitable for process monitoring in semiconductor manufacturing. Also called *monitor wafer*.

4.3.4 *virgin test wafer* — test wafer that has not been used previously in semiconductor manufacturing.

5 Ordering Information

5.1 Purchase orders for 2 inch, 3 inch, 100 mm, and 125 mm silicon test wafers furnished to this Specification shall include the items from the appropriate specification groups listed in Table 1.

Table 1 Wafer Classifications

<i>Classification</i>	<i>Applicable Specification Groups</i>
A	1, 2, 3
B	1, 2
C	1

5.2 Items which may be specified when ordering silicon wafers are listed in SEMI M18. Not all of these items are required for ordering test wafers. The following items are included in the three specification groups; numbers in square brackets following the item are the item numbers in SEMI M18:

5.2.1 *Group 1, General and Geometrical* — Growth method [1.1], diameter [6.1], surface orientation [6.9], thickness [6.7], orientation fiducials (flats and notches) [6.2–6.5], and edge profile [6.6].

5.2.2 *Group 2, Surface Characteristics* — Surface defects as listed in Tables 3 and 4 [7.1–7.2, 8.1–8.16].

5.2.3 *Group 3, Basic Intrinsic Properties* — Conductivity type [1.3], dopant [1.4], and resistivity [2.1].

5.3 Not all of the above items must be specified explicitly; the specifications for many of the items are determined by the combination of wafer classification and nominal diameter. In all cases, the following must be specified on the purchase order for all classes of 2 inch, 3 inch, 100 mm, and 125 mm test wafers.

5.3.1 Wafer Classification (A, B or C)

³ Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany;
<http://www.din.de>

⁴ Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: +81.3.3583.8005, Fax: +81.3.3586.2014,
<http://www.jsa.or.jp>

5.3.2 Nominal diameter and surface orientation

5.3.3 Growth method (see § 7)

5.3.4 Lot acceptance procedures (see § 9)

5.3.5 Certification (if required) (see § 12)

5.3.6 Packing and Marking (see § 13)

5.4 For Class A and B test wafers, that require controlled surface characteristics (see § 11), in addition to the items listed in § 5.3, see Table 4, §§ 8.1–8.16.

5.5 For Class A wafers, the following must be specified in addition to the items listed in §§ 5.3 and 5.4 (see § 8):

5.5.1 Conductivity type

5.5.2 Resistivity

5.6 Purchase Orders for 150 mm, 200 mm, and 300 mm silicon test wafers shall include the items from the appropriate specification groups listed in Table 2.

Table 2 Wafer Classifications

<i>Classifications</i>	<i>Applicable Specification Groups</i>
Mechanical	1
Process	1, 2

5.6.1 *Group 1, General and Geometrical* — Growth method [1.1], diameter [6.1], surface orientation [6.9], thickness [6.7], orientation fiducials (flats and notches) [6.2–6.5], and edge profile [6.6].

5.6.2 *Group 2, Surface and Intrinsic Properties* — Surface defects as listed in Table 3 [7.1–7.2, 8.1–8.16], conductivity type [1.3], dopant [1.4], and resistivity [2.1].

5.7 Not all the specifications must be specified explicitly; the specifications for many of the items are determined by wafer classification and nominal diameter. In all cases the following must be specified on the purchase order for all classes of 150 mm, 200 mm, and 300 mm test wafers:

5.7.1 Wafer Classification (*Mechanical* or *Process*)

5.7.2 Nominal diameter and surface orientation

5.7.3 Growth method (see § 7)

5.7.4 Lot acceptance procedures (see § 9)

5.7.5 Certification (if required) (see § 12)

5.7.6 Packing and Marking (see § 13)

6 Dimensions and Permissible Variations

6.1 The material shall conform to the parameters as specified in Tables 3 or 4.

6.2 If test wafers are specified to be edge contoured, the profile shall conform to the requirements in § 5.2 of SEMI M1 and to the dimension C_y in the associated polished silicon wafer standard applicable to the same nominal diameter and thickness. If edge profiling is not specified explicitly, there is no specification for the geometrical dimensions of any profiles which may exist on the wafers.

6.3 The material shall conform to the crystallographic orientation details as listed in the tables.

7 Materials and Manufacture

7.1 The material shall consist of wafers from crystals grown by the process specified in the purchase order or contract.

8 Electrical Requirements

8.1 The material shall conform to the details specified in the purchase order or contract, as follows:

8.1.1 Conductivity type

8.1.2 Resistivity

9 Sampling

9.1 Unless otherwise specified, ASTM E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) and lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

10 Test Methods

NOTE 1: Silicon wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

NOTE 2: The crystal growth method (e.g., Czochralski or Float Zone) and dopant (e.g., boron, phosphorous or antimony) used are difficult to ascertain in finished wafers. Verification test procedures for certification of these characteristics shall be agreed upon between the supplier and the purchaser.

10.1 *Diameter* — Determine in accordance with ASTM F613.

10.2 *Thickness, Center Point* — Determine in accordance with ASTM F533 or DIN 50441-1, or JIS H 0611.

10.3 *Flat Length* — Determine in accordance with ASTM F671.

10.4 *Flat Orientation* — Determine in accordance with ASTM F847.

10.5 *Surface Orientation* — Determine in accordance with ASTM F26 or DIN 50433.

10.6 *Surface Defects and Contamination* — Determine in accordance with ASTM F523. The following conditions shall be used (unless otherwise specified in the purchase or contract):

1. Background light intensity: 8 ± 2 fc (86 ± 22 lux)
2. Angle α (alpha): $45^\circ \pm 10^\circ$
3. Angle β (beta): $90^\circ \pm 10^\circ$

See § 11 for surface defect criteria and Table 2 for allowable levels of defects. In the event the wafers fail to meet these criteria, they shall be conditioned according to ASTM F612 or other cleaning procedure as agreed upon between supplier and user and retested.

NOTE 3: ASTM F154 is a useful guide for defining a variety of surface features found on silicon surfaces and for establishing commonly understood terms for describing them. It also gives detailed procedures for illumination and microscopical examination of surfaces.

10.7 *Conductivity Type* — Determine in accordance with ASTM F42 or DIN 50432.

10.8 *Resistivity* — Determine by methods agreed upon between the supplier and the purchaser.

NOTE 4: Resistivity of wafers is most appropriately determined for referee purposes by ASTM F84 or DIN 50431. Under some circumstances these tests may be considered destructive, and an alternative means may be required. A widely used nondestructive test is ASTM F673, having a range from 0.0001 to 200 $\Omega \cdot \text{cm}$.

10.9 *Radial Resistivity Variation* — Determine in accordance with ASTM F81 or DIN 50435.

10.10 *Crystal Perfection* — Determine in accordance with ASTM F47 or DIN 50434 (to determine grain boundaries, twinning, slip, dislocations, and lineage).

10.11 *Edge Profile* — Determine in accordance with ASTM F928 or DIN 50441-2.

11 Surface Defect Criteria

11.1 *Minimal Conditions or Dimensions* — The minimal conditions or dimensions for defects stated below shall be used for determining wafer acceptability. Anomalies smaller than these limits shall not be considered defects.

11.2 *Area Contamination* — Any foreign matter on the surface in localized areas which is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains, water spots, etc.

11.3 *Crack* — Any anomaly conforming to the definition and greater than 0.25 mm (0.010 in.) in total length.

11.4 *Crow's Foot* — Any anomaly conforming to the definition and greater than 0.25 mm (0.010 in.) in total length.

11.5 *Dimple* — Any smooth surface depression greater than 3 mm in diameter.

11.6 *Edge Chip and Indent* — Any edge anomaly including saw exit marks conforming to the definition and greater than 0.25 mm (0.010 in.) in radial depth and peripheral length.

11.7 *Hand Scribe Mark* — Any mark such as that caused by a diamond scribe that is visible under diffuse illumination.

11.8 *Haze* — Haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the polished wafer surface. (Under some conditions contamination may appear as haze.)

11.9 *Orange Peel* — Any roughened surface conforming to the definition that is observable under diffuse illumination.

11.10 *Particulate Contamination* — Distinct particles resting on the surface which are revealed under collimated light as bright points.

11.11 *Pit* — Any individually distinguishable non-removable surface anomaly conforming to the definition and visible when viewed under high intensity illumination.

11.12 *Saw Marks* — Any surface irregularities conforming to the definition that is observable under diffuse illumination.

11.13 *Scratch* — Any anomaly conforming to the definition and having a length-to-width ratio greater than 5:1.

11.14 *Slip* — Any pattern of short ridges aligned along $\langle 110 \rangle$ directions and visible under diffuse illumination.

11.15 *Striations* — Any helical features conforming to the definition and visible under diffuse illumination.

12 Certification

12.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this Specification, together with a report of the test results, shall be furnished at the time of shipment.

12.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as 'capable of meeting' certain requirements. In this context, 'capable of meeting' shall signify that the supplier is not required to perform the appropriate tests in § 10. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

13 Packing and Marking

13.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices, to provide ample protection against damage during shipment.

13.2 The wafers supplied under this Specification shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing.