SEMI M8-0306
SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON TEST WAFERS

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on January 16, 2006. Available at www.semi.org in March 2006; originally published in 1984; previously published July 2003.

NOTICE: This Document was completely rewritten in 2006.

SUPERSEDED

1 Purpose

1.1 This Specification covers requirements for virgin silicon test wafers to be used for mechanical testing, and routine process monitoring in semiconductor manufacturing.

2 Scope

2.1 This Specification covers dimensional and crystallographic properties of monocrystalline virgin silicon test wafers together with selected electrical and surface defect characteristic.

2.2 This Specification covers virgin test wafers in all standard wafer diameters from 2 inch to 300 mm. It classifies test wafers according to the items specified. It provides three classes of smaller diameter test wafers (through 125 mm), and two classes of larger diameter test wafers (from 150 mm).

2.3 This Specification does not cover test wafers intended for applications placing higher demands on silicon wafers, such as particle counting, measuring resolution in a photolithography process, or monitoring metallic contamination; for wafers to be used in these applications, the user should reference SEMI M24.

2.4 For referee purposes, U.S. customary units shall be used for wafers of 2- and 3-inch nominal diameter and System International (SI), commonly called metric units, for 100 mm and larger diameter wafers.

2.5 The complete EDI Code List for items in the Order Form appropriate to silicon wafers, including polished wafers, can be found in SEMI M18.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M45 — Provisional Specification for 300mm Wafer Shipping System

SEMI M59 — Terminology for Silicon Technology

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI Standards*[1]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

[1] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, http://www.ansi.org

Documents Document Sharing Hub

Full document details: SEMI M8-0306

ANSI/EIA 556-B — Outer Shipping Container Standard

3.3 *ASTM Standard*[2]

ASTM E122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Most general terms, acronyms, and symbols relating to silicon technology are defined in SEMI M59.

4.2 *Definitions* — The following definitions apply in the context of this Specification:

4.2.1 *mechanical test wafer* — silicon wafer suitable for testing equipment with emphasis on dimensional and structural characteristics only.

4.2.2 *process test wafer* — silicon wafer suitable for process monitoring as well as some processing applications in semiconductor manufacturing. Also called *monitor wafer*.

4.2.3 *virgin test wafer* — test wafer that has not been used previously in semiconductor manufacturing.

5 Ordering Information

5.1 Purchase orders for silicon test wafers furnished to this Specification shall include the appropriate order entry information from Table 1, Polished Wafer Specification Format for Order Entry, in SEMI M1. All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included:

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.8 Wafer Surface Orientation
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions
- 2-6.3 Primary Flat/Notch Orientation
- 2-6.6 Edge Profile
- 2-6.7 Thickness

Other items shall be included as agreed between supplier and customer.

5.2 In addition, the purchase order must indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

5.3 The parameter values provided in Tables 3, 4, and 5 may be used to identify appropriate values in the specification without selecting a value for each line.

5.4 For items in Tables 3, 4, and 5 that contain alternative specifications, the desired specification must be contained in the purchase order unless the supplier has the option of which specification to use.

5.5 Note that items that specify 'SEMI M1' generally need to be further specified because SEMI M1 frequently has several values for such items.

5.6 The following items must also be included in the purchase order:

5.6.1 Lot acceptance procedures

5.6.2 Certification (if required)

5.6.3 Packing and shipping container labeling requirements

[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, http://www.astm.org

SUPERSEDED

Documents
Document Sharing Hub

Full document details: SEMI M8-0306

5.6.4 Wafer classification (A,B, or C in Table 1, Mechanical or Process in Table 2).

5.7 The appropriate classifications are listed in Tables 1 and 2.

5.7.1 *Small Diameter Test Wafers (2 inch, 3 inch, 100 mm and 125 mm)* — The following items are included in the three specification groups shown in Table 1; numbers in square brackets following the item are the item numbers in SEMI M1:

5.7.1.1 *Group 1*, *General and Geometrical* — Growth method [2-1.1], diameter [2-6.1], wafer surface orientation [2-1.8], thickness [2-6.7], fiducial dimensions (flats and notches) [2-6.2–2-6.5], and edge profile [2-6.6].

5.7.1.2 *Group 2, Surface Characteristics* — Surface defects as listed in Tables 3, 4, and 5 [2-7.1–2-7.3, 2-8.1–2-8.17].

5.7.1.3 *Group 3, Basic Intrinsic Properties* — Conductivity type [2-1.4], dopant [2-1.5], and resistivity [2-2.1].

Table 1 Classifications for Small Diameter Wafers: (2 inch, 3 inch, 100 mm, and 125 mm)

Classification	*Applicable Specification Groups*
A	Gr 1; General and Geometrical + Gr 3; Basic Intrinsic Properties
B	Gr 1; General and Geometrical + Gr 2; Surface Characteristics
C	Gr 1; General and Geometrical

5.7.2 Large Diameter Test Wafers (150 mm, 200 mm, and 300 mm): The following items are included in the two specification groups shown in Table 2; numbers in square brackets following the item are the item numbers in SEMI M1.

5.7.2.1 *Group 1, General and Geometrical* — Growth method [2-1.1], diameter [2-6.1], wafer surface orientation [2-1.8], thickness [2-6.7], fiducial dimensions (flats and notches) [2-6.2–2-6.5], and edge profile [2-6.6].

5.7.2.2 *Group 2, Surface and Intrinsic Properties* — Surface defects as listed in Table 3 [2-7.1–2-7.3, 2-8.1–2-8.17], conductivity type [2-1.4], dopant [2-1.5], and resistivity [2-2.1].

Table 2 Wafer Classifications for Large Diameter Wafers: (150 mm, 200 mm, and 300 mm)

Classifications	*Applicable Specification Groups (Gr)*
Mechanical	Gr 1, General and Geometrical
Process	Gr 1, General and Geometrical + Gr2, Surface and Intrinsic Properties

6 Requirements

6.1 Tables 3, 4, and 5 provide Specifications for Polished Monocrystalline Silicon Test Wafers for 2 inch, 3 inch, 100 mm, 125 mm, 150 mm, 200 mm, and 300 mm Diameter. A parameter not listed in these tables need not be specified.

6.2 It is also essential to specify appropriate test methods in each case. Defaults for test method selection are given in ¶ 8.

NOTE 1: The line items with numbers beginning with '2-' are listed in Part 2 of the Silicon Wafer Specification Format for Order Entry , SEMI M1, Table 1.

7 Sampling

7.1 Unless otherwise specified, ASTM Practice E122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified

SUPERSEDED

Documents Document Sharing Hub
Full document details: SEMI M8-0306

in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between the supplier and customer.

8 Test Methods

8.1 Measurements shall be made or certifiable to one of the SEMI, ASTM, JEITA, JIS, or DIN standard test methods for the item as selected from the Silicon Wafer Specification Format for Order Entry, Part 2, located in Table 1 of SEMI M1, and specified in the purchase order.

8.2 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

8.3 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method shall be a method in common usage for the region of the purchaser of the wafer.

8.4 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

8.5 Information about the various test methods cited is provided in Related Information 2 of SEMI M1 together with information about some additional test methods no longer in wide use throughout the industry.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this Specification, together with a report of test results shall be furnished at the time of shipment.

9.2 In the interest of controlling inspection costs, the supplier and the customer may agree that the material shall be certified as 'capable of meeting' with certain requirements. In this context, 'capable of meeting' shall signify that the supplier is not required to perform the appropriate tests in § 8. However, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Product Labeling

10.1 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one month after that particular lot has been accepted by the customer.

10.2 Alternatively, if agreed upon between supplier and customer, one of the box labeling schemes in SEMI T3 shall be used and the information listed in ¶ 10.1 that is not included on the label shall be retained in the supplier's database for at least one month after that particular lot has been accepted by the customer.

10.3 Wafers of 300 mm diameter shall be shipped in packages labeled in accordance with SEMI M45.

11 Packing and Shipping Container Labeling

11.1 Special packing requirements shall be subject to agreement between the supplier and the customer. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices, to provide ample protection against damage during shipment.

11.2 Wafers of 300 mm diameter shall be shipped in accordance with SEMI M45.

11.3 Unless otherwise indicated in the purchase order, all outside wafer shipping containers shall be labeled in accordance with ANSI/EIA 556-B.

SUPERSEDED

Documents
Document Sharing Hub
Full document details: SEMI M8-0306