

SEMI M8-0703

SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON TEST WAFERS

This Standard was technically approved by the Silicon Wafer Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on April 11, 2003. Available at www.semi.org in July 2003; originally published in 1984; previously published March 2001.

NOTICE: This Document was completely rewritten in 2003.

1 Purpose

1.1 This Specification covers requirements for virgin silicon test wafers to be used for mechanical testing, and routine process monitoring in semiconductor manufacturing.

2 Scope

2.1 This Specification covers dimensional and crystallographic properties of monocrystalline virgin silicon test wafers together with selected electrical and surface defect characteristic.

2.2 This Specification covers virgin test wafers in all standard wafer diameters from 2 inch to 300 mm. It classifies test wafers according to the items specified. It provides three classes of smaller diameter test wafers (through 125 mm), and two classes of larger diameter test wafers (from 150 mm).

2.3 This Specification does not cover test wafers intended for applications placing higher demands on silicon wafers, such as particle counting, measuring resolution in a photolithography process, or monitoring metallic contamination; for wafers to be used in these applications, the user should reference SEMI M24.

2.4 For referee purposes, U.S. customary units shall be used for wafers of 2- and 3-inch nominal diameter and SI (System International), commonly called metric units, for 100 mm and larger diameter wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

3.2 ASTM Standard¹

ASTM F1241 — Standard Terminology of Silicon Technology

3.3 Other Standards

A comprehensive list of applicable standard test methods from a variety of sources is given in Table 1 of SEMI M18.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions of terms related to silicon wafer technology are given in ASTM Terminology F1241.

4.2 Definitions for some additional relevant terms are given in SEMI M1.

¹ ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>

4.3 The following definitions apply in the context of this Specification:

4.4 Definitions

4.4.1 *mechanical test wafer* — silicon wafer suitable for testing equipment with emphasis on dimensional and structural characteristics only.

4.4.2 *process test wafer* — silicon wafer suitable for process monitoring as well as some processing applications in semiconductor manufacturing. Also called *monitor wafer*.

4.4.3 *virgin test wafer* — test wafer that has not been used previously in semiconductor manufacturing.

5 Ordering Information

5.1 Small Diameter Wafers

5.1.1 Items that may be specified when ordering silicon wafers are listed in SEMI M18. Not all of these items are required for ordering small diameter (2 in., 3 in., 100 mm, and 125 mm) test wafers. The following items are included in the three specification groups shown in Table 1; numbers in square brackets following the item are the item numbers in SEMI M18:

5.1.1.1 *Group 1, General and Geometrical* — Growth method [1.1], diameter [6.1], surface orientation [6.9], thickness [6.7], orientation fiducials (flats and notches) [6.2–6.5], and edge profile [6.6].

5.1.1.2 *Group 2, Surface Characteristics* — Surface defects as listed in Tables 3 and 4 [7.1–7.2, 8.1–8.16].

5.1.1.3 *Group 3, Basic Intrinsic Properties* — Conductivity type [1.3], dopant [1.4], and resistivity [2.1].

Table 1 Classifications for Small Diameter Wafers

<i>Classification</i>	<i>Applicable Specification Groups</i>
A	1, 2, 3
B	1, 2
C	1

5.1.2 Not all of the above items must be specified explicitly; the specifications for many of the items are determined by the combination of wafer classification and nominal diameter. In all cases, the following must be specified on the purchase order for all classes of small diameter test wafers:

5.1.2.1 Wafer Classification (A, B or C),

5.1.2.2 Nominal diameter and surface orientation,

5.1.2.3 Growth method (see ¶ 7.1),

5.1.2.4 Lot acceptance procedures (see ¶ 9.1),

5.1.2.5 Certification (if required) (see § 12),

5.1.2.6 Packing and Marking (see § 13),

5.1.2.7 Any options listed in the table, and

5.1.2.8 Appropriate test methods when more than one is listed for the parameter in Table 1 of SEMI M18.

5.1.3 For Class A and B test wafers, that require controlled surface characteristics, certain surface defect limits (see § 11), must be specified in addition to the items listed in ¶ 5.1.2, see Table 3, Sections 8.1–8.16.

5.1.4 For Class A wafers, the following must be specified in addition to the items listed in ¶¶ 5.1.2 and 5.1.3 (see ¶ 8.1):

5.1.4.1 Conductivity type

5.1.4.2 Resistivity

5.2 Large Diameter Wafers

5.2.1 Items that may be specified when ordering silicon wafers are listed in SEMI M18. Not all of these items are required for ordering large diameter (150 mm, 200 mm, and 300 mm) test wafers. The following items are included in the two specification groups shown in Table 2; numbers in square brackets following the item are the item numbers in SEMI M18.

Table 2 Wafer Classifications for Large Diameter Wafers

<i>Classifications</i>	<i>Applicable Specification Groups</i>
Mechanical	1
Process	1, 2

5.2.1.1 *Group 1, General and Geometrical* — Growth method [1.1], diameter [6.1], surface orientation [6.9], thickness [6.7], orientation fiducials (flats and notches) [6.2–6.5], and edge profile [6.6].

5.2.1.2 *Group 2, Surface and Intrinsic Properties* — Surface defects as listed in Table 3 [7.1–7.2, 8.1–8.16], conductivity type [1.3], dopant [1.4], and resistivity [2.1].

5.2.2 Not all the specifications must be specified explicitly; the specifications for many of the items are determined by wafer classification and nominal diameter. In all cases the following must be specified on the purchase order for all classes of large diameter test wafers:

5.2.2.1 Wafer Classification (*Mechanical* or *Process*),

5.2.2.2 Nominal diameter and surface orientation,

5.2.2.3 Growth method (see ¶ 7.1),

5.2.2.4 Lot acceptance procedures (see ¶ 9.1),

5.2.2.5 Certification (if required) (see § 12),

5.2.2.6 Packing and Marking (see § 13),

5.2.2.7 Any options listed in the table, and

5.2.2.8 Appropriate test methods when more than one is listed for the parameter in Table 1 of SEMI M18.

6 Dimensions and Permissible Variations

6.1 The material shall conform to the parameters as specified in Table 3, 4, or 5.

6.2 If test wafers are specified to be edge contoured, the profile shall conform to the requirements in § 5.2 of SEMI M1 and to the dimension C_y in the associated polished silicon wafer standard applicable to the same nominal diameter and thickness. If edge profiling is not specified explicitly, there is no specification for the geometrical dimensions of any profiles that may exist on the wafers.

6.3 The material shall conform to the crystallographic orientation details as listed in the tables.

7 Materials and Manufacture

7.1 The material shall consist of wafers from crystals grown by the process specified in the purchase order or contract.

8 Electrical Requirements

8.1 Class A test wafers and process test wafers (only) shall conform to the details specified in the purchase order or contract, as follows:

8.1.1 Conductivity type

8.1.2 Resistivity

9 Sampling

9.1 Unless otherwise specified, ASTM E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) and lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

10 Test Methods

NOTE 1: Silicon wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

NOTE 2: The crystal growth method (for example, Czochralski or Float Zone) and dopant (e.g., boron, phosphorous or antimony) used are difficult to ascertain in finished wafers. Verification test procedures for certification of these characteristics shall be agreed upon between the supplier and the purchaser.

10.1 Use test methods for the specified quantities as listed in Table 1 of SEMI M18.

11 Surface Defect Criteria

11.1 *Minimal Conditions or Dimensions* — The minimal conditions or dimensions for defects stated below shall be used for determining wafer acceptability. Anomalies smaller than these limits shall not be considered defects.

11.2 *Area Contamination* — Any foreign matter on the surface in localized areas which is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains, water spots, etc.

11.3 *Crack* — Any anomaly conforming to the definition and greater than 0.25 mm (0.010 in.) in total length.

11.4 *Crow's Foot* — Any anomaly conforming to the definition and greater than 0.25 mm (0.010 in.) in total length.

11.5 *Dimple* — Any smooth surface depression greater than 3 mm in diameter.

11.6 *Edge Chip and Indent* — Any edge anomaly including saw exit marks conforming to the definition and greater than 0.25 mm (0.010 in.) in radial depth and peripheral length.

11.7 *Hand Scribe Mark* — Any mark such as that caused by a diamond scribe that is visible under diffuse illumination.

11.8 *Haze* — Haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the polished wafer surface. (Under some conditions contamination may appear as haze.)

11.9 *Orange Peel* — Any roughened surface conforming to the definition that is observable under diffuse illumination.

11.10 *Particulate Contamination* — Distinct particles resting on the surface, which is revealed under, collimated light as bright points.

11.11 *Pit* — Any individually distinguishable non-removable surface anomaly conforming to the definition and visible when viewed under high intensity illumination.

11.12 *Saw Marks* — Any surface irregularities conforming to the definition that is observable under diffuse illumination.

11.13 *Scratch* — Any anomaly conforming to the definition and having a length-to-width ratio greater than 5:1.

11.14 *Slip* — Any pattern of short ridges aligned along <110> directions and visible under diffuse illumination.

11.15 *Striations* — Any helical features conforming to the definition and visible under diffuse illumination.

12 Certification

12.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this Specification, together with a report of the test results, shall be furnished at the time of shipment.