

SEMI M83-0820

TEST METHOD FOR DETERMINATION OF DISLOCATION ETCH PIT DENSITY IN MONOCRYSTALS OF III-V COMPOUND SEMICONDUCTORS

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1 Purpose

1.1 The purpose of this Document is to specify a test method for determination of the dislocation etch pit density of monocrystals and wafers of the III-V compound semiconductors GaAs, InP and GaP.

2 Scope

2.1 This Test Method covers the determination of dislocation etch pit density on round test slices and commercial wafers of III-V compound semiconductors using optical microscopy for identification and registration of dislocation etch pits.

2.2 The dislocation etch pit density is used as a measure for the dislocation density or the crystallographic perfection of a crystal.

2.3 This Test Method describes methods for preparation of slices and wafers of the III-V compound semiconductors GaAs, InP, and GaP with {100} or {111} surfaces by structural etching. These etching procedures are performed to reveal dislocations by formation of etch pits on the surface of the test specimens.

2.4 The described methods for identification and registration of etch pits as well as the procedures for evaluation can be applied also to monocrystalline semiconductor slices or wafers of other materials or orientations, provided that there are suitable structural etching procedures available.

2.5 This Test Method is applicable to material with dislocation densities up to $200,000 \text{ cm}^{-2}$. The resistivity and conductivity type of the material is irrelevant.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M10 — Terminology for Identification of Structures and Features Seen on Gallium Arsenide Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

NOTE 1: Refer to SEMI's Compilation of Terms (COTs) for a list of the most current terms and their definitions.

4.1 Terms, acronyms, and symbols relating to compound semiconductor material technology are defined in SEMI M10 and SEMI M59.

4.2 Other Definitions Used in this Test Method

4.2.1 *dislocation etch pit density (EPD)* — the number of dislocation etch pits per unit area.

4.2.2 *measurement field* — a rectangular area of the surface of the test specimen for which a local value of the dislocation etch pit density is determined.

4.2.3 *measurement location* — the center of the measurement field specified by coordinates or an index which refers to a measurement location plan.

4.2.4 *measurement location plan* — list of measurement locations for which measurements of local EPD are performed.

4.2.5 *off-orientation* — deviation of a crystal surface from a crystallographic plane, characterized by an angle ϕ (see SEMI MF26) and a direction of tilt, which is given by the projection of a vector normal to the crystal surface onto the referenced crystallographic plane.

4.2.6 *saucer pit* — a shallow etch pit in a crystal surface with no clearly recognizable bottom point, indicating other types of crystal lattice defects instead of dislocations.

5 Summary of Test Method

5.1 In this Test Method dislocation etch pit density in monocrystals of III-V compound semiconductors is determined as a measure for the dislocation density.

5.2 Test specimens for this method are wafers or slices of monocrystals with surfaces with a deviation from the $\{100\}$ or $\{111\}$ crystallographic reference plane by an angle ϕ of at most 15° or 6° , respectively.

5.3 Rough surfaces of etch specimens are flattened by polish-etching with specific etchants.

5.4 The test specimens are etched with an etchant specific for the semiconductor material. On the surfaces of test specimens etch pits of characteristic shape are formed at the intersection points of dislocation lines with the surface.

5.5 The number of etch pits within certain measuring fields is determined by counting using an optical microscope. The number and position of measuring positions is defined by a measurement location plan.

5.6 The etch pit density is calculated as the number of etch pits per area unit.

6 Physical Background

6.1 When the surface of a test specimen is treated by the etching techniques according to this Test Method, distinctive etch pits of characteristic shapes will result at the intersections of dislocation lines with the surface.

6.2 Etching of $\{100\}$ surfaces of GaAs generates elongated hexagonal etch pits (see Figure 1a), while on $\{100\}$ surfaces of InP and GaP approximately rectangular etch pits appear (see Figures 1b and 1c). The side-walls of etch pits correspond to low-index planes of the crystal lattice. They converge towards a common bottom point. This bottom point is a characteristic feature of dislocation etch pits and allows a discrimination from other etching features.

6.3 On test specimens with $\{111\}$ surfaces form and size of etch pits will be different on front and back surface due to the chemical polarity of these surfaces. The etch pits on $\{111\}$ surfaces exhibit a triangular shape due to the symmetry conditions of this lattice plane. For GaAs it is recommended to choose the $\{111\}$ As surface for EPD measurement because of the more clearly developed etch pits (see Figure 1d).

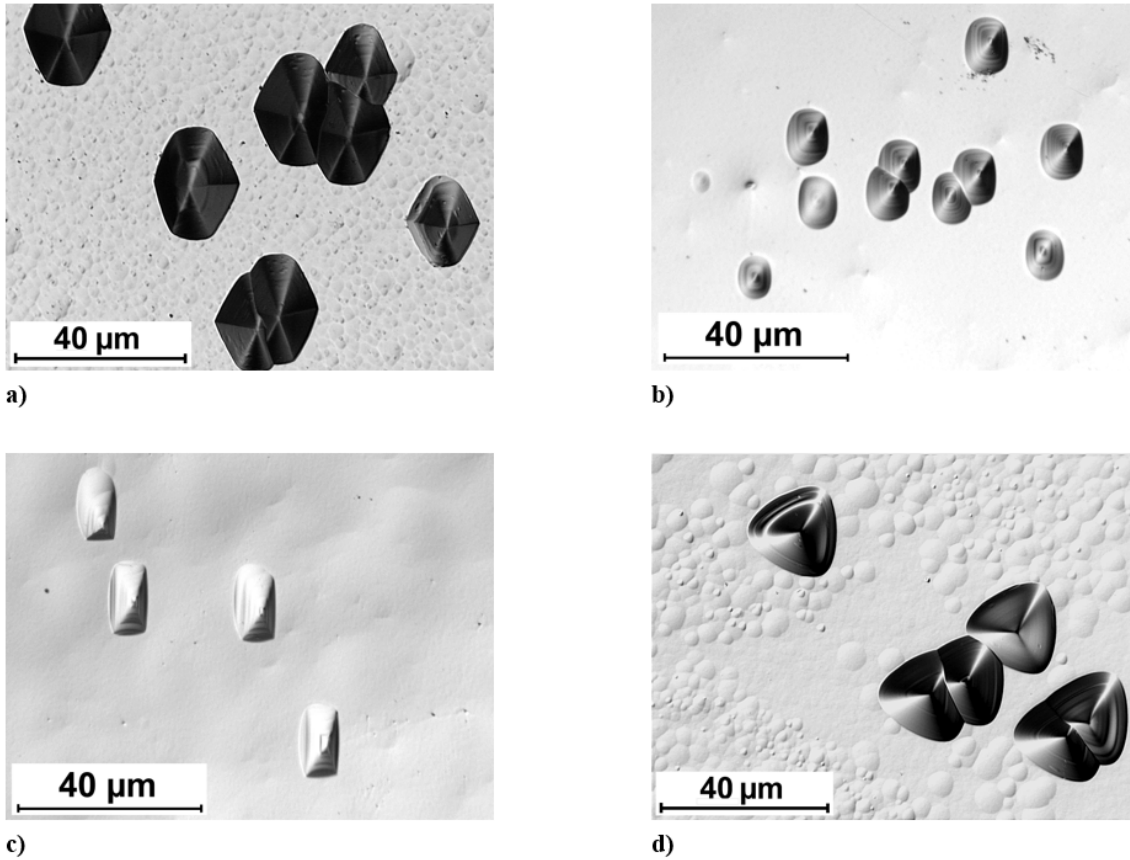


Figure 1
Microscopical Images of Dislocation Etch Pits on Surfaces of Different III-V Compound Semiconductor Materials: {100} GaAs (a), {100} InP (b), {100} GaP (c), and {111} GaAs (d)

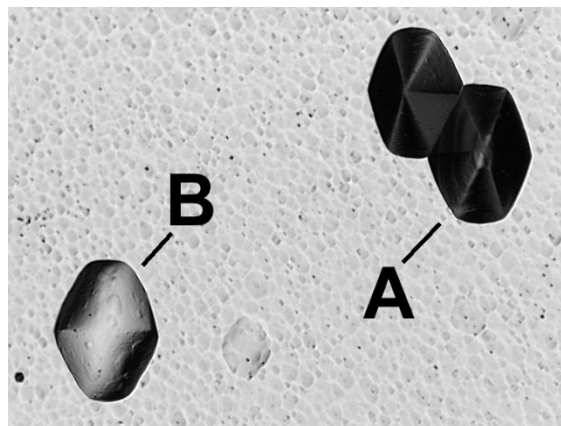


Figure 2
Dislocation Etch Pit (A) and Saucer Pit (B) on a {100} GaAs Surface

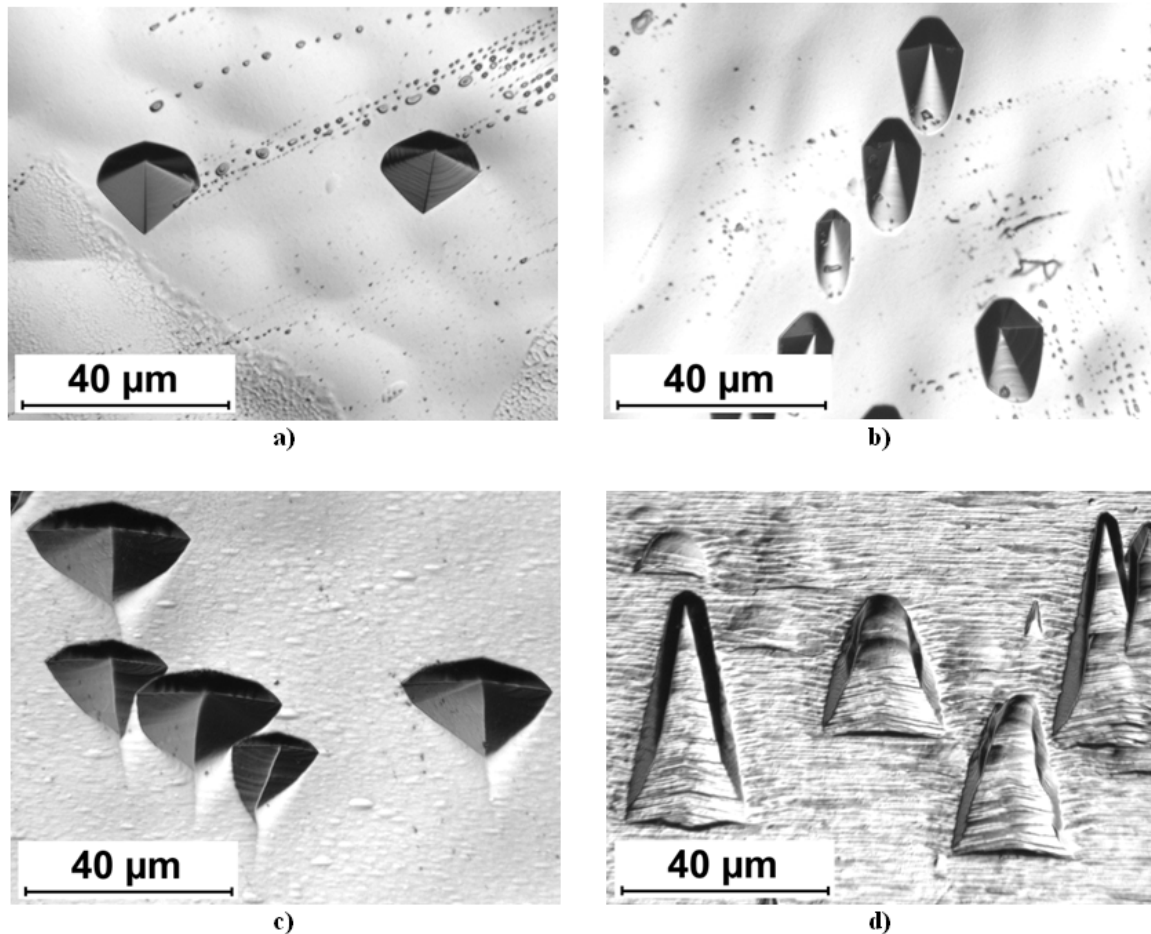


Figure 3

Microscopical images of dislocation etch pits on GaAs surfaces with an off-orientation from the {100} crystallographic plane of 6° (a, b) and 15° (c, d). The off-orientation is directed towards the {111}Ga face (a, c) or the {111}As face (b, d). The distortion of the shape of etch pits due to off-orientation of the sample surface is stronger in the case of tilt towards the {111}As face. It is recommended to use that side of a wafer for EPD measurement which shows etch pits as in a) and c).

6.4 Besides dislocations other defects, such as point defects, precipitates and mechanical damage can cause the formation of etch pits. The resulting etch pits can be distinguished from dislocation etch pits by the missing bottom point (see Figure 2).

6.5 Only dislocations propagating on crystallographic planes perpendicular to the crystallographic reference plane will generate dislocation etch pits when using the etching techniques described in this Test Method. This means, that for example, dislocations on {111} planes will not be detected by etching a {100} surface. For this reason the etch pit density may systematically underestimate the dislocation density of a specific test specimen. If the identification of other types of dislocation is required, additional characterization methods must be applied, such as x-ray topography or cathodoluminescence topography.

6.6 On surfaces deviating from the crystallographic reference plane (off-orientated surfaces) the shape of dislocation etch pits changes depending on angle and direction of off-orientation (see Figure 3).

6.7 As demonstrated in Figure 3 for {100}GaAs, the distortion is stronger if the surface is tilted towards a {111}As face direction as compared to a tilt towards a {111}Ga face direction. For other III-V semiconductors a similar influence of tilt direction is observed. In the case of strong distortion of shape, as shown in Figure 3d, a reliable identification of etch pits is impossible. Because of the symmetry properties of the zinc blende structure of III-V