

SEMI M84-0414^E (Reapproved 0923) SPECIFICATION FOR POLISHED SINGLE CRYSTAL SILICON WAFERS FOR GALLIUM NITRIDE-ON-SILICON APPLICATIONS

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and §§) the symbols are used to reference more than one section or paragraph, respectively.

NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

1.1 Single crystal (monocrystalline) silicon wafers are utilized for essentially all integrated circuits and many other semiconductor devices. Gallium nitride on single crystal silicon wafers represents emerging markets with applications such as high brightness-light emitting diodes (HB-LED) or high-frequency power devices. At present, the specifications for silicon wafer substrates requested by customers of such wafers differ widely. To permit common processing and metrology equipment to be used in multiple device fabrication lines, it is essential for key wafer properties to be standardized. These Specifications provide the essential dimensions and certain other common characteristics of polished single crystal silicon wafers for gallium nitride-on-silicon applications.

1.2 Because both applications require the full range of thickness and edge profile specifications, there is no distinction between the two types of applications in these Specifications.

2 Scope

2.1 These Specifications cover ordering information and certain requirements for high-purity, single crystal polished silicon wafers used for gallium nitride-on-silicon applications.

2.2 Specifications for dimensional characteristics and selected other properties are provided for three types of single crystal polished silicon wafers:

- 150 mm flatted polished single crystal silicon wafers with secondary flat,
- 150 mm flatted polished single crystal silicon wafers without secondary flat, and
- 200 mm notched polished single crystal silicon wafers.

NOTE 1: Including 300 mm diameter notched polished single crystal silicon wafers now is premature; these types of wafers may be included in a future revision.

2.2.1 Values given for thickness, total thickness variation (TTV), bow, and warp apply only to wafers prior to application of back surface films, extrinsic gettering treatments, or other thermal treatments.

2.3 These Specifications apply specifically to prime silicon wafers with at least one chemical-mechanically polished surface. Ground, lapped, and unpolished wafers are not covered in these specifications but they may provide guidance in connection with their procurement.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M40 — Guide for Measurement of Surface Roughness of Planar Surfaces on Silicon Wafer

SEMI M59 — Terminology for Silicon Technology

SEMI T3 — Specification for Wafer Box Labels

3.2 ANSI® Standards¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 ASTM® Standards²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specific Precision, the Average for a Characteristic of a Lot or Process

3.4 MHIA Standard³

CEA 556-C — Outer Shipping Container Bar Code Label Standard

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59.

5 Ordering Information

5.1 Purchase orders for polished silicon wafers for GaN-on-silicon applications furnished to this Specification shall include all the order entry information from SEMI M1 Table 1, Polished Wafer Specification Format for Order Entry, Part 1, General Information, and the following information from Part 2, Substrates.

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity
- 2-5.1 Wafer ID Marking
- 2-5.7 Edge surface condition
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, <http://www.ansi.org>. ANSI trademark is owned by American National Standards Institute.

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

³ Material Handling Industry of America, 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA; Telephone: +1.704.676.1190, Fax: +1.704.676.1199, <http://www.mhia.org>

- 2-6.3 Primary Flat/Notch Orientation
- 2-6.4 Secondary Flat Length
- 2-6.5 Secondary Flat Location
- 2-6.6 Edge Profile
- 2-6.7 Thickness (center point)
- 2-6.8 Total Thickness Variation (max)
- 2-6.9 Bow, Absolute (max)
- 2-6.10 Warp (max)
- 2-8.5 Localized Light Scatterers (LLS)

5.2 Wafer categories are provided for various thicknesses of wafers. If a wafer category is specified on a purchase order, all the properties in Part 1 of the various tables in § 6 need not be specified independently, but all such properties must have the same values as in the table.

5.3 Other properties from Part 2 of Table 1 in SEMI M1 may also be specified if the application of the wafers requires them.

5.4 In addition, the purchase order must indicate the test method to be used in evaluating each of the specified properties for which alternate test procedures exist.

5.5 The following items must also be included in the purchase order:

- 5.5.1 Lot acceptance procedures,
- 5.5.2 Certification (if required), and
- 5.5.3 Packing and shipping container labeling requirements.

6 Requirements for Specifying Polished Single Crystal Silicon Wafers for GaN-on-Si Applications

6.1 150 mm Diameter Polished Single Crystal Silicon Wafers for GaN-on-Si Applications

6.1.1 Several types of 150 mm diameter single crystal single-side polished silicon wafers are commonly used for GaN-on-Si applications. General characteristics, electrical characteristics, chemical characteristics, structural characteristics, wafer preparations characteristics are described in SEMI M1.

6.1.2 It is essential to specify appropriate test methods in each case. Defaults for test method selection are given in § 8.

6.1.3 Tables 1 and 2 provide requirements for specifying dimensional characteristics and wafer ID marking requirements for 150 mm diameter silicon wafers. The property numbers in the left column of both tables are taken from SEMI M1 Table 1 Silicon Wafer Specification Format for Order Entry, Part 2 Substrate. All of the parameters listed in the table should be included in the purchase order contract.

Table 1 Requirements for 150 mm Polished Single Crystal Silicon Wafers with Secondary Flat for Gallium Nitride on Silicon Applications

Part 1: Standardized Specifications

Property		150 mm Wafers		
		1.8.GN1	1.8.GN2	1.8.GN3
2-6.1	Diameter	150.00 ± 0.20 mm		
2-6.2	Primary Flat Length	57.5 ± 2.5 mm		
2-6.3	Primary Flat Orientation ^{#1}	{110} ± 1°		
2-6.4	Secondary Flat Length	37.5 ± 2.5 mm		