

# SEMI M86-0915

## SPECIFICATION FOR POLISHED MONOCRYSTALLINE c-PLANE GALLIUM NITRIDE WAFERS

This Standard was technically approved by the Compound Semiconductor Materials Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on July 6, 2015 Available at [www.semiviews.org](http://www.semiviews.org) and [www.semi.org](http://www.semi.org) in September 2015.

### Table of Contents

|                                             |    |
|---------------------------------------------|----|
| 1 Purpose .....                             | 1  |
| 2 Scope .....                               | 3  |
| 3 Referenced Standards and Documents .....  | 3  |
| 4 Terminology .....                         | 4  |
| 5 Ordering Information.....                 | 5  |
| 6 Requirements.....                         | 6  |
| 6.1 General Characteristics .....           | 6  |
| 6.2 Electrical Characteristics .....        | 6  |
| 6.3 Structural Characteristics .....        | 6  |
| 6.4 Wafer Preparation Characteristics ..... | 6  |
| 6.5 Dimensional Characteristics .....       | 7  |
| 7 Sampling.....                             | 7  |
| 8 Test Methods .....                        | 7  |
| 9 Certification.....                        | 7  |
| 10 Packaging and Marking .....              | 8  |
| 11 Related Standards and Documents .....    | 8  |
| Appendix 1 Tables.....                      | 10 |
| Appendix 2 Figures .....                    | 15 |

### List of Tables

|                                                                                                                                                    |    |
|----------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Table A1-1 Common Properties.....                                                                                                                  | 10 |
| Table A1-2 Electrical Requirements.....                                                                                                            | 10 |
| Table A1-3 Polished Wafer Defect Limits .....                                                                                                      | 10 |
| Table A1-4 Dimensions and Coordinates of Points A to D for Edge Profile Template .....                                                             | 11 |
| Table A1-5 Dimensional and Tolerance Characteristics of 1-inch, 2-inch, 3-inch and 100-mm Gallium Nitride Wafers with Optional Secondary Flat..... | 12 |
| Table A1-6 Test Methods for GaN Wafer Specification and Order Entry .....                                                                          | 13 |
| Table A1-7 Orientation and Flat Location Requirements.....                                                                                         | 14 |

### List of Figures

|                                                                              |    |
|------------------------------------------------------------------------------|----|
| Figure A2-1 Fixed Quality Area.....                                          | 15 |
| Figure A2-2 Orthogonal Misorientation.....                                   | 15 |
| Figure A2-3 Depth and Length of Edge Chip and Indent.....                    | 15 |
| Figure A2-4 Flat Length of Primary Orientation Flat and Secondary Flat ..... | 16 |

|                                                                                                                                                                                   |    |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Figure A2-5 Relation of Lattice Sites, Crystallographic Planes and Flats (flat length not to scale) The Position of the Secondary Flat is Shown for View on the Gallium Face..... | 16 |
| Figure A2-6 SEMI Wafer Edge Profile Template .....                                                                                                                                | 17 |
| Figure A2-7 Examples of Acceptable and Unacceptable Wafer Edge Profiles .....                                                                                                     | 17 |

SUPERSEDED

## 1 Purpose

1.1 This Specification covers substrate requirements for monocrystalline high-purity c-plane (0001) gallium nitride wafers used in semiconductor electronic and optical device manufacturing.

## 2 Scope

2.1 A complete purchase specification may require the defining of additional physical, electrical, and bulk properties. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

2.2 This Specification is directed specifically to c-plane (0001) gallium nitride wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find this Specification helpful in defining their requirements. Hereafter, the term 'gallium nitride wafers' will refer to 'c-plane (0001) gallium nitride wafers.'

2.3 The material is single crystal c-plane gallium nitride (GaN). The following properties in Table A1-1 are listed for use as guidelines:

2.4 For referee purposes, SI (System International, commonly called metric) units shall be used.

2.5 Dimensional requirements are provided for the following categories of polished wafers:

- Category 1.1 25.4 mm Round Polished Monocrystalline Gallium Nitride Wafers
- Category 1.2 50.8 mm Round Polished Monocrystalline Gallium Nitride Wafers
- Category 1.3 76.2 mm Round Polished Monocrystalline Gallium Nitride Wafers
- Category 1.4 100.0 mm Round Polished Monocrystalline Gallium Nitride Wafers

**NOTICE:** SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

## 3 Referenced Standards and Documents

### 3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF43 — Test Methods for Resistivity of Semiconductor Materials

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning (Withdrawn 0914)

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI T5 — Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers

### 3.2 ASTM Standards<sup>1</sup>

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specified Precision, the Average for Characteristic of a Lot or Process

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

### 3.3 ASQ Standard<sup>2</sup>

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

### 3.4 JIS Standard<sup>3</sup>

JIS H 0611 — Methods of Measurement of Thickness, Taper and Bow for Silicon Wafers

**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

## 4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M59.

### 4.1 Definitions

4.1.1 *bow* — of a semiconductor wafer, a measure of concave or convex deformation of the median surface of a wafer, independent of any thickness variation which may be present. Bow is the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer. Unit of bow is generally micrometers.

4.1.2 *crystallite* — any part of the wafer, having an arbitrary orientation of its crystallographic axis in respect to the monocrystalline part of the wafer.

4.1.3 *curvature of lattice* — curvature of the principle crystal plane associated with the intended epitaxial surface of the wafer, which may differ from the surface bow described in ¶ 4.1.1. Lattice curvature consists of the orientation change of the normal of this crystal plane as a function of position on the wafer. It must be measured using X-ray diffraction (e.g., via multiple on-axis rocking curve scans), and is typically expressed as a radius of curvature, typically expressed in units of m.

4.1.4 *dopant* — a chemical element, usually from the second, fourth or sixth column of the periodic table for the case of III-V compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.5 *edge contouring* — on wafers whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the wafer joining the front and back sides.

4.1.6 *edge exclusion* — the width  $X$  of a narrow band of wafer surface, located just inside the wafer edge, over which the values of the specified parameter do not apply. See definition of *fixed quality area* below.

4.1.7 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal edge exclusion,  $X$ , over which the specified values of a parameter apply.

4.1.7.1 *Discussion* — The boundary of the FQA is at all points the distance  $X$  away from the periphery of a wafer of nominal dimensions (see Figure A2-1). The size of the FQA is independent of wafer diameter and flat length tolerances.

4.1.8 *inversion domains* — isolated three-dimensional regions in the GaN wafer having inverted polarity with respect to the rest of the crystal.

<sup>1</sup> ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: 610.832.9585, Fax: 610.832.9555, <http://www.astm.org>

<sup>2</sup> American Society for Quality, 600 North Plankinton Avenue, Milwaukee, WI 53203, USA; Telephone: 414.272.8575, Fax: 414.272.1734, <http://www.asq.org>

<sup>3</sup> Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014; <http://www.jsa.or.jp>

4.1.9 *lot* — for the purpose of this Document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.10 *orthogonal misorientation* — in {0001} wafers cut intentionally ‘off-orientation’, the angle between the projection of the vector normal to the wafer surface onto the {0001} plane and the projection on that plane of the specified direction of tilt in the {0001} plane (see Figure A2-2).

4.1.11 *screw dislocation (SD)* — a line defect in the crystalline lattice in which the Burgers vector is parallel to the dislocation line, specifically  $l = [0001]$  and  $b = [0001]$ . Therefore for (0001)-oriented GaN, screw dislocations propagate approximately perpendicular to the surface normal.

4.1.12 *surface orientation* — the tilt angle between the crystallographic c-axis and the wafer surface normal (see Figure A2-2).

4.1.13 *threading dislocation (TD)* — a class of crystalline line defects including edge, screw and mixed (both edge and screw) types. Threading dislocations are classified by their propagation direction with respect to the Burgers vector. Screw dislocations propagate parallel to the Burgers vector (typically  $l=b=[0001]$ ), edge dislocations propagate perpendicular to the Burgers vector (typically  $l=[0001]$ ,  $b=1/3\langle 2-1-10 \rangle$ ), and mixed dislocations contain both an edge and screw component.

4.1.14 *total indicator reading (TIR)* — the smallest perpendicular distance between two planes, both parallel with respect to the reference plane, which encloses all points on the front surface of a wafer within the FQA, the site, or the subsite, depending on which is specified. TIR is generally expressed in micrometers.

4.1.15 *total thickness variation (TTV)* — the difference between the maximum and minimum thickness values of a wafer encountered during a scan pattern or a series of point measurements. TTV is generally expressed in micrometers.

4.1.16 *v-pit* — a small depression in a c-plane GaN wafer surface with a symmetrical inverted pyramidal shape featuring six facets and a width-to-height ratio near 1. This is also known as an inverted hexagonal pyramid (IHP), or a hexagonal pinhole. When a V-pit or an IHP is formed, a hexagonal region of the (0001) surface is replaced with six (101-1) sidewall facets.

4.1.17 *warp* — of a semiconductor slice or wafer, the difference between the most positive and most negative distances of the median surface of a free, unclamped wafer from a reference plane, encountered during a scan pattern. Warp is a bulk property of the test specimen, not a property of an exposed surface. Warp is generally expressed in micrometers.

## 5 Ordering Information

5.1 Purchase orders for gallium nitride wafers furnished to this Specification shall include the following items:

5.1.1 Nominal Diameter (see Table A1-5),

5.1.2 Thickness (see Table A1-5),

5.1.3 Dopant (this property depends strongly on the quickly evolving technology and suitable limits for a standard do not exist),

5.1.4 Resistivity or Carrier Concentration (see Table A1-2),

5.1.5 Conductivity Type,

5.1.6 TTV (see Table A1-5),

5.1.7 Surface Orientation (see Table A1-7),

5.1.8 Polarity of the Front (device) Surface—gallium-plane or nitrogen-plane,

5.1.9 Lot Acceptance Procedures (see § 8),

5.1.10 Certification (see § 9), and

5.1.11 Packing and Marking (see § 11).

## 6 Requirements

### 6.1 General Characteristics

6.1.1 The crystal growth method shall be one of the following: hydride vapor phase epitaxy (HVPE), ammonothermal growth, Na-flux, and similar solution-based techniques.

### 6.2 Electrical Characteristics

6.2.1 Proposed electrical requirements are shown in Table A1-2. These properties depend strongly on the quickly evolving technology and need to be negotiated between vendor and user.

### 6.3 Structural Characteristics

#### 6.3.1 Standard Defect Limits

6.3.1.1 The material shall conform to the dimensions and dimensional tolerances as specified in Table A1-5.

6.3.1.2 The material shall conform to the crystallographic orientation details as specified in Table A1-7.

6.3.1.3 Flats shall conform to the requirements of § 6.4.1.

#### 6.3.2 Surface Defects (see Figure A2-3 and Table A1-3)

6.3.2.1 Minimal conditions or dimensions for surface defects are stated below. These limits shall be used for determining wafer acceptability; anomalies smaller than these limits shall not be considered as defects.

##### 6.3.2.2 Surface Defect Definitions

6.3.2.2.1 *Edge Chip and Indent* — Any edge anomaly including saw exit marks conforming to the definition [ASTM F154] and greater than 0.25 mm in radial depth and peripheral length.

6.3.2.2.2 *Orange Peel* — Any visually detectable roughened surface conforming to the definition [SEMI MF154] and observable under diffused illumination. Pits with a spacing of less than 2 mm are treated as orange peel.

6.3.2.2.3 *Particles* — Distinct particles resting on the surface which are revealed under collimated intense light as bright points.

6.3.2.2.4 *Pit* — Any individually distinguishable depression in the surface with a length-to-width ratio smaller than 5:1, visible when viewed under intense illumination.

6.3.2.2.4.1 This definition is different from SEMI MF154 in so far as the slope of the sides of the depression are not taken into account.

6.3.2.2.5 *Scratch* — Any anomaly conforming to the definition [SEMI MF154] and having a length-to-width ratio greater than 5:1 and visible under intense illumination.

##### 6.3.3 Bulk Defects Definitions

6.3.3.1 *Crack* — Any anomaly conforming to the definition [SEMI MF154] and greater than 0.25 mm in total length.

6.3.3.2 *Crystallite* — Any anomaly conforming to the definition (see § 4) and having a misorientation of more than 1° to the main (monocrystalline) part of the wafer and having a maximum width larger than 0.20 mm.

6.3.3.3 *V-Pit* — Any anomaly conforming to the definition (see § 4) having a maximum width larger than 10 µm.

### 6.4 Wafer Preparation Characteristics

#### 6.4.1 Wafer Flat System

6.4.1.1 For gallium nitride wafers with the surface normal close to the crystallographic c-axis (small tilt angles, see Figure A2-2) one primary orientation flat and one optional secondary flat is specified. The primary flat always has a greater flat length compared to the secondary flat (see Figure A2-4).

6.4.1.2 The angle between primary and optional secondary flat is always 90° (see Figure A2-5). For the tolerance see Table A1-7.