SEMI M9-0211
SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE SLICES

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1 Purpose

1.1 These specifications cover two groups of substrate requirements for monocrystalline high-purity gallium arsenide wafers used in semiconductor and electronic device manufacture. Dimensional and crystallographic orientation characteristics and limits on surface defects are the only standardized properties set forth below.

2 Scope

2.1 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

2.2 These specifications are directed specifically to gallium arsenide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.3 The material is single crystal gallium arsenide (GaAs) having a cubic zinc blende structure and having the following properties. The following properties are for use as guidelines:

Density	5.316 gm/cm^3
Melting Point	1238°C
Dielectric Constant	13.1
Lattice Parameter	5.654 Å
Energy Gap	1.42 eV

2.4 For reference purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards*

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

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3.2 *ANSI Standard*[1]

ANSI/ASQ Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standards*[2]

ASTM E122 — Practice for Calculating Sample Size to Estimate, With Specified Precision, the Average for a Characteristic of a Lot or Process

ASTM F76 — Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single-Crystal Semiconductors

ASTM F613 — Test Method for Measuring Diameter of Semiconductor and Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Definitions*

4.1.1 *bow* — of a semiconductor slice or wafer, a measure of concave or convex deformation of the median surface of a slice or wafer, independent of any thickness variation which may be present. Bow is a bulk property of the test specimen, not a property of an exposed surface. Generally, bow is determined with a test specimen in a free, unclamped condition. Units of bow are generally micrometers or inches.

4.1.2 *dopant* — a chemical element, usually from the second, fourth, or sixth columns of the periodic table for the case of III-V compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.3 *edge contouring* — on slices whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the slice joining the front and back sides.

4.1.4 *flat diameter* — the linear dimension across the surface of a semiconductor wafer from the center of the flat through the wafer center to the circumference of the wafer on the opposite edge along the diameter perpendicular to the flat. (See Figure 6.)

NOTE 1: The flat diameter may be associated with the primary orientation flat, with a secondary flat, if present, or with any other flat, if present. In such cases, the terms may be modified as primary orientation flat diameter, secondary flat diameter, etc.

4.1.5 *lot* — for the purpose of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.6 *orthogonal misorientation* — in {100} wafers cut intentionally "off-orientation," the angle between the projection of the vector normal to the slice surface onto the {100} plane and the projection on that plane of the nearest direction. (See Figure 5.)

4.1.7 *total thickness variation (TTV)* — the difference between the maximum and minimum thickness values of a slice or wafer encountered during a scan pattern or a series of point requirements. TTV is generally expressed in micrometers or mils (thousandths of an inch).

4.1.8 *warp* — of a semiconductor slice or wafer, the difference between the maximum and minimum distances of the median surface of the slice or wafer from a reference plane, encountered during a scan pattern. Warp is a bulk property of the test specimen, not a property of an exposed surface. Warp is generally expressed in micrometers or mils (thousandths of an inch).

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[2] American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; http://www.astm.org

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5 Ordering Information

5.1 Purchase orders for gallium arsenide wafers furnished to this specification shall include the following items:

5.1.1 Nominal diameter (see applicable SEMI Standard for polished GaAs wafers),

5.1.2 Thickness (see applicable SEMI Standard for polished GaAs wafers),

5.1.3 Total Thickness Variation (see applicable SEMI Standard for polished GaAs wafers),

5.1.4 Surface orientation (see applicable SEMI Standard for polished GaAs wafers). There are two options of flat location for 2 inch and 3 inch diameter polished monocrystalline GaAs wafers for integrated circuit and optoelectronic applications. They are V-Groove (as illustrated in Figure 1 and Figure 3) and Dove-Tail (as illustrated in Figure 2 and Figures 4). These designations describe the shape of groove that can be etched perpendicular to the primary flat.

5.1.5 The following are the options of wafer surface orientation:

A. (100) ± 0.5° as shown in Figure 1 and Figure 2.

B. For V-Groove option: (100) off 2° toward the (110) plane which is located between the primary and secondary flats as shown in Figure 3. Figure 5 illustrates orthogonal misorientation.

C. For Dove-Tail option: (100) off 2° toward any of the nearest (110) planes as shown in Figure 4. Figure 5 illustrates orthogonal misorientation.

5.1.6 Lot Acceptance Procedures (see § 8),

5.1.7 Certification (see § 11),

5.1.8 Packing and Marking (see § 12).

5.2 *Optional Criteria* — The following items may be specified optionally in addition to those listed above:

5.2.1 Crystal Growth Method,

5.2.2 Etch Pit Density (EPD) of Crystal,

5.2.3 Crystal Growth Perfection,

5.2.4 Impurity Type,

5.2.5 Surface Condition of Wafer,

5.2.6 Edge Contour,

5.2.7 Mobility,

5.2.8 Resistivity,

5.2.9 Carrier Concentration,

5.2.10 Thermal Conversion Characteristics.

6 Dimensions and Permissible Variations

6.1 The material shall conform to the dimensions and dimensional tolerances as specified in the applicable polished gallium arsenide slice standard.

6.2 If edge contoured wafers are specified on the purchase order, the profile shall conform to the following requirements at all points on the wafer periphery.

6.2.1 When the wafer is aligned with the SEMI Wafer Edge Profile Template (see Figure 6) so that the x-axis of the template is coincident with the wafer surface and the y-axis of the template is tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template (see Figure 7 for example of acceptable and unacceptable contours).

6.2.2 No sharp points or protrusions are permitted anywhere on the wafer edge contour.

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6.2.3 Cosmetic attributes of the edge contour are not covered by this specification. They shall be agreed upon between supplier and purchaser.

7 Materials and Manufacture

7.1 The material shall consist of wafers from ingots grown to the material definition specified in the purchase order or contract.

8 Physical Requirements

8.1 The material shall conform to the crystallographic orientation details as specified in the applicable polished gallium arsenide slice standard.

8.2 The material shall conform to the details specified in the purchase order or contract as follows:

8.2.1 Conduction Type,

8.2.2 Dopant,

8.2.3 Carrier Concentration,

8.2.4 Resistivity,

8.2.5 Thermal Conversion Characteristics,

8.2.6 Etch Pit Density,

8.2.7 Mobility,

8.2.8 Surface Characteristics,

8.2.9 Growth Methods.

9 Sampling

9.1 Unless otherwise specified, ASTM E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQ Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4 definitions for critical, major and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

10 Test Methods

10.1 *Diameter* — Determined by ASTM F613.

10.2 *Thickness, Center Point* — Determined by SEMI MF533.

NOTE 2: GaAs wafers are extremely fragile. While the mechanical dimensions of a slice can be measured by use of tools such as a micrometer calipers and other conventional techniques, the slice may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

10.3 *Flat Length* — Determined by SEMI MF671.

10.4 *Flat Orientation* — Determined by etching method identified in the appropriate polished GaAs wafer standard.

10.5 *Bow and Warp* — Determine bow in accordance with SEMI MF534 and warp in accordance with SEMI MF657.

10.6 *Total Thickness Variation* — Determined by SEMI MF533 or SEMI MF657.

10.7 *Surface Orientation* — Determined by SEMI MF26.

10.8 *Orthogonal Misorientation* — Determined by a method agreed upon between the supplier and purchaser.

10.9 *Surface Defects and Contamination* — Determined by a method agreed upon between the supplier and purchaser.

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