

SEMI M92-0423

SPECIFICATION FOR 4H-SiC HOMOEPITAXIAL WAFER

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and §§) the symbols are used to reference more than one section or paragraph, respectively.

NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

- 1.1 This Specification covers requirements for 4H-SiC homoepitaxial wafers used in power device manufacturing.
- 1.2 This Specification provides a uniform standard of 4H-SiC homoepitaxial wafers for the suppliers and the customers in the industrial chain.

2 Scope

2.1 This Specification specifies the parameters of 4H-SiC homoepitaxial wafers with a single epitaxial layer grown on an *n*-type substrate, up to and including 30 µm total thickness.

2.2 Dimensional requirements are provided for the following categories of epitaxial wafers:

- 100.0 mm 4H-SiC epitaxial wafers
- 150.0 mm 4H-SiC epitaxial wafers

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Polished Wafers

SEMI M55 — Specification for Polished Monocrystalline Silicon Carbide Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI M81 — Guide to Defects Found on Monocrystalline Silicon Carbide Substrates

SEMI M83 — Test Method for Determination of Dislocation Etch Pit Density in Monocrystals of III-V Compound Semiconductors

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers By Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafer by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ASTM® Standards*¹

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With a Specified Tolerable Error, the Average for Characteristic of a Lot or Process

3.3 *ASQ® Standards*²

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M1, SEMI M55, and SEMI M59.

4.1 *Abbreviations and Acronyms*

4.1.1 *GBIR* — global flatness back surface ideal range

4.1.2 *SBIR* — site flatness back surface ideal range

4.2 *Definitions*

4.2.1 *area contamination* — any foreign matter on the surface in localized areas that is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains or waters, etc.

4.2.2 *buffer layer* — a transition layer epitaxially-formed between a substrate and the first epitaxial layer.

4.2.3 *crack* — cleavage or fracture that extends to the surface of a wafer.

4.2.4 *dislocation* — a line imperfection in a crystal lattice that is characterized by a closure failure of Burgers' circuit that may form the boundary between slipped and non-slipped areas of a crystal or occur at the edge of stacking faults or around precipitates.

4.2.5 *dislocation etch pit* — a pit generated by a preferential etch where a dislocation meets the surface of a wafer.

4.2.6 *downfall* — a macroscopic size particle existing within or extending beyond the epitaxial layer. The crystal structure of the particles is usually 3C.

4.2.7 *edge chip* — region where material has been unintentionally removed from the edge of the wafer.

4.2.8 *edge exclusion (EE)* — the distance from the fixed quality area (FQA) boundary to periphery of a wafer of nominal dimensions.

4.2.9 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal EE, over which the specified values of a parameter apply. Because the nominal EE relates to the nominal diameter of a wafer, the size of the FQA is independent of wafer diameter and flat length tolerances.

¹ ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

² The American Society for Quality, 600 North Plankinton Avenue, Milwaukee, WI 53203, USA; Telephone: +1.800.248.1946, Fax: +1.414.272.1734, <http://www.asq.org>. ASME trademark is owned by The American Society for Quality.

4.2.10 *global flatness back surface ideal range (GBIR)* — a parameter of flatness.

4.2.10.1 *Discussion* — Refer to SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as ‘total thickness variation (TTV)’.

4.2.11 *homoepitaxial layer* — thin monocrystalline film epitaxially-formed on a substrate of the same material and crystallographic orientation, inheriting the atomic order of the substrate.

4.2.12 *micropipe* — small hollow tube basically parallel to the crystallographic c-axis and extending typically through larger parts of the crystal boule and thus affecting several neighboring wafers. Micropipes may be generated at bulk defects, for example, inclusions, polytype defects or crystallites. (Refer to SEMI M81 for examples.)

4.2.13 *polytype* — one of the modifications of monocrystalline material which shows polytypism.

4.2.14 *polytypism* — phenomenon where a material occurs in several structural modifications, each of which can be regarded as built up by stacking layers of identical structure and chemical composition.

4.2.15 *site flatness back surface ideal range (SBIR)* — a parameter of flatness.

4.2.15.1 *Discussion* — Refer to SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as ‘local thickness variation (LTV or LTVmax)’.

4.2.16 *scratch* — a shallow groove or cut below the established plane of the surface of a semiconductor wafer, with a length to width ratio greater than 5:1.

4.2.17 *silicon carbide (SiC)* — semiconductor crystal composed of silicon and carbon, which will exhibit a large number of polytypes such as 3C, 4H, 6H, and 15R.

NOTE 2: A symbol like 4H- gives the number of periodic stacking bilayers (2, 3, 4...) and the crystal symmetry (H = hexagonal, C = cubic, and R = Rhombohedral) of each polytype.

4.2.18 *substrate* — a wafer that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuits that may be fabricated directly in the substrate or in a film of the same or another material grown or deposited on the substrate.

4.2.19 *surface killer defect* — surface killer defects of 4H-SiC epitaxial wafers caused by epitaxial growth are including downfall, triangular defect and carrot defect.

4.2.20 *total usable area* — the proportion of the area of the wafer without surface killer defects to the area of the entire wafer.

4.2.21 *triangular defect* — a triangle-shaped defect on the 4H-SiC epitaxial layer surface, which is a lamellar inclusion with a cubic (3C) stacking sequence, so-called ‘3C inclusion’, extending toward the epitaxial layer surface.

5 Ordering Information

5.1 Purchase orders for 4H-SiC epitaxial wafers furnished to this Specification shall include the following items from substrate, buffer layer and epitaxial layer. In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist. Special requirements of ordering information shall be agreed upon between the supplier and the purchaser.

5.2 Substrate

5.2.1 Substrate Vendor,

5.2.2 Crystal Polytype,

5.2.3 Conductivity Type,

5.2.4 Dopant,

5.2.5 Diameter,

5.2.6 Thickness,

5.2.7 Wafer Surface Orientation,

5.2.8 Resistivity,