SEMI MF1153-1110 (Reapproved 0222)
TEST METHOD FOR CHARACTERIZATION OF METAL-OXIDE-SILICON (MOS) STRUCTURES BY CAPACITANCE-VOLTAGE MEASUREMENTS

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (¶) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and ¶¶) the symbols are used to reference more than one section or paragraph, respectively.

1 Purpose

1.1 Net carrier density present near the silicon-oxide interface may constitute an important acceptance requirement. Where there is not significant compensation by impurities of the opposite conductivity type, the material resistivity may be determined from this carrier density using SEMI MF723.

1.2 Flatband voltage is an important parameter in the manufacture of MOS devices. Its value is dependent on the work function difference between the silicon and the metal field plate, interface trapped charge, and fixed or trapped charge distributed within the oxide. It can be an indicator of anomalies in these values.[1]

1.3 Instability of the flatband voltage of an MOS structure subjected to voltage stress at elevated temperatures is a measure of the mobile ionic charge density within the oxide. Most device applications require that mobile ionic charge be minimized.

1.4 The presence of unwanted subsurface *p-n* junctions may have deleterious effects on device operation.

1.5 This Test Method may be employed for qualification of furnaces or other semiconductor device-processing equipment where such qualification depends on the determination of contamination resulting from high mobile ionic charge density.

1.6 This Test Method covers measurement of metal-oxide-silicon (MOS) structures for flatband capacitance, flatband voltage, average carrier density within a depletion length of the semiconductor-oxide interface, displacement of flatband voltage after application of voltage stress at elevated temperatures, mobile ionic charge contamination, and total fixed charge density. Also covered is a procedure for detecting the presence of *p-n* junctions in the subsurface region of bulk or epitaxial silicon.

2 Scope

2.1 This Test Method is applicable to *n*-type and *p*-type bulk silicon with carrier density from 5×10^{14} to 5×10^{16} carriers per cm^3, inclusive, and n/n^+ and p/p^+ epitaxial silicon with the same range of carrier density.

2.2 This Test Method is applicable for test specimens with oxide thicknesses of 50 to 300 nm.

2.3 This Test Method can give an indication of the density of defects within the MOS structure. These defects include interface trapped charge, fixed oxide charge, trapped oxide charge, and permanent inversion layers.

2.4 This Test Method is applicable for measurement of mobile ionic charge density of 1×10^{10} cm^{-2} or greater. Alternative techniques, such as the triangular voltage sweep method,[2] may be required where mobile ionic charge density less than 1×10^{10} cm^{-2} must be measured.

[1] Sze, S. M., *Physics of Semiconductor Devices*, Wiley-Interscience, New York (1981): pp. 379–402.

[2] Kuhn, M., and Silversmith, D. J. "Ionic Contamination and Transport of Mobile Ions in MOS Structures." *J. Electrochem. Soc.* **118**, 996 (1971).

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2.5 This Test Method is applicable for measurement of total fixed charge density of 5×10^{10} cm^{-2} or greater. Alternative techniques, such as the conductance method,[3] may be required where the interface trapped-charge density component of total fixed charge of less than 5×10^{10} cm^{-2} must be measured.

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3 Limitations

3.1 If the apparatus is not well shielded from electromagnetic interference caused by radio frequency (r-f) fields, their presence may affect the measurements because the impedance of the MOS structure is high and because the test signal used is in the mV range.

3.2 The presence of any light during the measurements adversely affects the results because the capacitance of the MOS device in the inversion condition is light sensitive.

3.3 The measurement may be affected if the relative humidity of the environment is permitted to exceed 60%. The use of dry nitrogen gas flowing into the sample chamber is recommended to control excess humidity.

3.4 The presence of a permanent surface inversion layer condition can affect the measurement.

NOTE 1: A permanent surface inversion layer condition (refer to Figure 1) makes it difficult to determine the value for equilibrium minimum capacitance C_{min} to be used in the calculations. If an incorrect C_{min} were chosen, all shift values would still be correct, but dopant density and fixed charge density computations would be wrong.

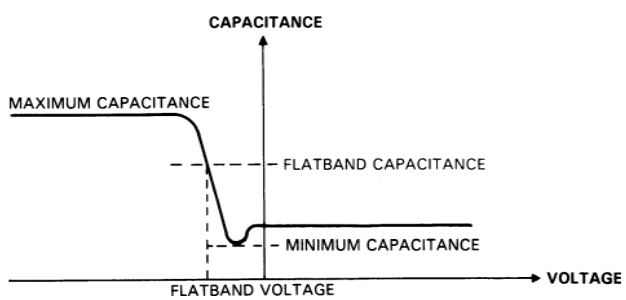

Figure 1
Capacitance-Voltage Plot of MOS Device Fabricated with *p*-Type Silicon Showing the Minimum Dip of a Permanent Inversion Layer

3.5 Stray capacitance and inductance caused by excessive lengths of connecting cable and by improper zeroing of the capacitance measuring instrument can cause significant errors in the capacitance measurement. Typical cable lengths shall be kept below 1 m.

3.6 Alternating current, (AC) test signals greater than 25 mV RMS can lead to errors in the measured capacitance.

3.7 Series resistance between the MOS capacitor and the capacitance-measuring instrument can cause significant errors in the measured capacitance. Sources of series resistance can be in the sample itself, in the back contact, or in the test cables.

3.8 A leaky oxide that draws significant current can cause errors in the measured capacitance.

3.9 Inability of an inversion layer to form in an MOS sample precludes measurement by this test method.

3.10 Very long minority-carrier lifetime in an MOS sample may cause errors in the measurement of C_{min} if the inversion layer has not had sufficient time to form.

[3] Nicollian, E. H., and Goetzberger, A. "The SiO_2 Interface–Electrical Properties as Determined by the MIS Conductance Technique." *Bell Syst. Tech. J.* **46**, 1105 (1967).

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NOTE 2: A maximum lifetime cannot be specified readily. However, an error will occur if the lamp in ¶ 11.9 is not illuminated for sufficient duration, or is not of sufficient intensity to generate charge to form the inversion layer.

3.11 Prolonged negative-bias temperature stressing can result in a shift in flatband voltage larger than the shift due to mobile ionic charge alone.

3.12 Hysteresis in the capacitance-voltage characteristics of an MOS sample can cause significant error in the determination of mobile ionic charge density.

3.13 The precision of this Test Method can be affected by inhomogeneities in the oxide or in the semiconductor parallel to the semiconductor-oxide interface.

4 Referenced Standards and Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI M59 — Terminology for Silicon Technology

SEMI MF576 — Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry

SEMI MF723 — Practice for Conversion Between Resistivity and Dopant or Carrier Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Acronyms, terms, and symbols related to silicon technology, including those used in this Test Method, are listed and defined in SEMI M59.

5.2 Definitions of terminology for oxide charges associated with thermally oxidized silicon have been standardized in the literature.[4]

6 Summary of Test Methods

6.1 A specimen MOS structure consisting of a metal field plate on the oxidized silicon substrate is fabricated.

6.2 The small-signal, high-frequency capacitance of the specimen is measured as a function of a ramped voltage applied between the field plate and the silicon substrate.

6.3 The surface carrier density, flatband capacitance, and flatband voltage, are computed from the capacitance and voltage data.

6.4 A voltage stress is applied to the sample at elevated temperature and the shift in V_{fb} is measured after cooling. This shift is interpreted as a measure of the density of mobile ionic charges in the oxide.

6.5 Total fixed-charge density is calculated from the flatband voltage.

6.6 The presence of subsurface *p-n* junctions is detected by photosensitivity. The specimen is biased into accumulation, and the capacitance measured and recorded. The specimen is then illuminated and the capacitance remeasured. An increase in capacitance due to illumination is interpreted as an indication of the presence of a *p-n* junction.

6.7 Light generates charge in the *p-n* junction and alters the capacitance of the junction that is in series with the MOS device. For the purposes of this Test Method, the subsurface region is defined as the region extending from the true surface to a depth at which no light penetrates. For the visible spectrum, maximum penetration depth is the penetration depth associated with the longest wavelength in the spectral distribution of the light source, which has the smallest absorption coefficient.

[4] Deal, B. E. "Standardized Terminology for Oxide Charges Associated with Thermally Oxidized Silicon." *IEEE Trans. Electron Devices,* **ED-27**, 605 (1980).

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7 Apparatus

7.1 *Facilities* — For growing gate quality oxides and for depositing and defining metal field plates on the oxide.

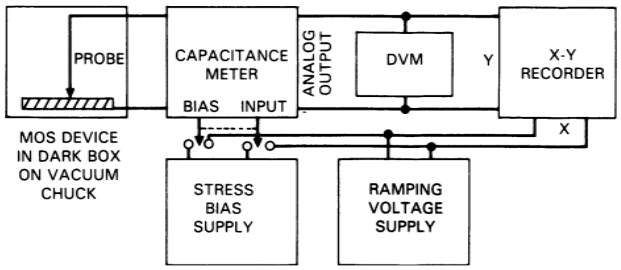

Figure 2
Capacitance-Voltage Measurement Circuit

7.2 *Electrical Apparatus (refer to Figure 2)*

7.2.1 *Ramping DC Voltage Supply* — Covering the range ±100 V and capable of sweeping between any two preset voltages within that range. Sweeping rate shall be variable between 0.1 and 1 V/s. Ripple shall be 0.5% of the DC output, or less. The supply shall be capable of supplying a fixed preset voltage with an accuracy of ±10 mV.

7.2.2 *Capacitance Meter* — With full scale ranges of 1 to 1000 pF, or greater, in decade, or smaller, steps. The measurement frequency shall be in the range 0.9 to 1.1 MHz inclusive. The accuracy shall be 0.5% of full scale or better for each range and the reproducibility shall be 0.25% of full scale or better. The instrument shall be capable of sustaining an external DC bias of ±100 V or greater and shall be capable of compensating for an external probe fixture with stray capacitance of up to 5 pF. The AC measuring signal shall be 0.025 V RMS or less. The meter shall have an analog voltage output proportional to the capacitance measurement; output impedance shall be 100 Ω, or less.

NOTE 3: C-V measurements of MOS capacitors built from thin oxides on high resistivity substrates exhibit high series resistance effects which may require concurrent conductance measurements and subsequent computations to determine the true MOS capacitance. This test method is limited to capacitance-only measurements, but includes a test in ¶ 12.1 to check for the presence of series resistance effects.

7.2.3 *Digital Voltmeter (DVM)* — With sensitivity 1 µV or better, accuracy of 0.5% of full scale or better, a reproducibility of 0.25% of full scale or better, an input impedance of 10 MΩ or greater, and a common mode rejection 100 dB or greater at 60 Hz.

7.2.4 *X-Y Recorder* — With a minimum slewing speed of 20 cm/s, an accuracy of 0.5% of full scale or better, a linearity of 0.5% of full scale or better, and an input impedance of 1 MΩ or greater. *X*-axis and *y*-axis sensitivities shall be 5 mV/cm or greater.

7.2.5 *Stress Bias DC Power Supply* — Capable of supplying 0 to ±100 V (open circuit) with ripple 1% of the DC output or less, to be used for voltage stressing.

7.3 *Standard Capacitors* — Of accuracy 0.25% or better at the measurement frequency. At least one capacitor shall be used for each capacitance meter range used. At least one capacitor shall be in the range 1 to 10 pF inclusive and one shall be in the range 10 to 100 pF inclusive.

7.4 *Probe Fixture*

7.4.1 *Probe* — To contact the top field plate; probe force shall not exceed 1.75 N; probe tip shall have a nominal radius of curvature of 5 µm; probe and holder shall be designed such that the stray capacitance is less than 1 pF.

7.4.2 *Vacuum Chuck* — To hold the specimen wafer and contact the back surface; capable of reaching a temperature of 300°C, and maintaining set temperature to within ±10°C over the specimen area.

7.4.3 *Light Tight Metal Box* — To enclose the specimen during the measurement. Equipped with incandescent lamp, 7 to 20 W.

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