

SEMI MF1388-0707 (Reapproved 1023) TEST METHOD FOR GENERATION LIFETIME AND GENERATION VELOCITY OF SILICON MATERIAL BY CAPACITANCE-TIME MEASUREMENTS OF METAL-OXIDE-SILICON (MOS) CAPACITORS

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (¶) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and ¶¶) the symbols are used to reference more than one section or paragraph, respectively.

NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

1.1 Generation lifetime and generation velocity are strongly influenced by electrically active deep-level impurities and physical imperfections in the silicon, and are thus an indication of the quality of the silicon wafer. Such electrically active deep-level impurities and physical imperfections can cause excessive *p-n* junction leakage, poor dynamic random access memory (RAM) refresh performance, and ‘dark current’ degradation in computer-controlled display (CCD) memories, delay lines, filters, and imagers.

NOTE 1: The lifetime measured by this Test Method is that of the processed material, not necessarily that of the virgin silicon. Extreme care needs to be taken to ensure that such aspects of metal-oxide-silicon (MOS) capacitor fabrication as pre-oxidation clean, process gases, chemicals, and furnace quartzware do not introduce lifetime altering contaminants (also refer to ¶ 3.3.3).

1.2 This Test Method is suitable for monitoring the generation lifetime and generation velocity of silicon wafers in the following situations:

1.2.1 *Incoming and Outgoing Inspection of Silicon Wafers* — Due to the length of measurement time at room temperature and destructive nature of the test, such inspection should be restricted to a small number of wafers. In the absence of an interlaboratory evaluation of the precision of this Test Method, its use for materials acceptance is not recommended unless the parties to the test mutually agree on the method's repeatability and on the correlation they can obtain.

1.2.2 *Contamination Monitoring of Processing Equipment, Materials, or Procedures* — Such monitoring requires using silicon wafers of known generation lifetime and generation velocity, obtained from lots sampled by previous MOS capacitance-time characterization, to fabricate the MOS capacitors. The results can then be compared to the known material values to determine the effect of the processing. Due to variations in generation lifetime and generation velocity of typical groups of silicon wafers, a large number of measurements may be required to produce statistically significant results.

1.2.3 *Research and Development Purposes* — For the evaluation of new materials, processes, and methods involved in the fabrication of semiconductor devices.

2 Scope

2.1 This Test Method covers the measurement of generation lifetime and generation velocity of silicon wafers.

2.2 The measurement requires the fabrication of a guard-ring MOS capacitor (refer to Figure 1). This Test Method is therefore destructive to the silicon wafer.

2.3 This Test Method may also be applied to semiconductor materials other than silicon and to insulators other than silicon dioxide, but the details of capacitor fabrication and the analyses and interpretation of data in such cases are not given in this Test Method.

2.4 Both *p*- and *n*-type silicon in the dopant density range from 10^{13} cm^{-3} to 10^{17} cm^{-3} can be evaluated by this Test Method. The approximate range of generation lifetime that can be measured is 1 μs to 10 ms.

2.5 The Test Method is applicable to both bulk and epitaxial silicon. If epitaxial silicon is used, the epitaxial layer must be of the same conductivity type as the substrate and should be at least twice as thick as the maximum depletion width in deep depletion to avoid errors caused by the proximity of the epitaxial interface (refer to ¶ 12.4).

2.6 It is necessary to complete the measurements described in SEMI MF1153 before performing the measurements described in this Test Method to determine the values of maximum capacitance, equilibrium minimum capacitance, and dopant density.

2.7 A digital computer capable of controlling the instruments and recording data is required and significantly simplifies and improves the accuracy of the data acquisition and analysis process.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 *Instrumentation Errors* — Typical errors due to instrumentation include the following sources:

3.1.1 *Stray Capacitance, Inductance, Conductance, Resistance, and Phase Errors* — Such errors are caused by excessive lengths of connecting cable between the capacitance meter and the measurement fixture. Carefully review and follow the capacitance meter or bridge manufacturer's recommendations regarding cable length and necessary correction factors.

3.1.2 *Improper Compensation of Stray Capacitance, Inductance, Conductance, and Resistance Associated with the Measurement Fixture* — Such errors can cause the calculated value of the generation lifetime to increase, and in excessive cases, cause the calculated lifetime to be negative.

3.1.3 *Poor Bias Stability* — Any disturbance in bias during the measurement results in errors. Some commercially available capacitance meters and bridges drop their internal bias supplies to zero volts during autoranging, causing errors in the capacitance-time characteristic.

3.2 *Measurement Fixture and Enclosure Errors* — Typical errors due to the measurement fixture and enclosure include the following sources:

3.2.1 *Poor Temperature Stability* — Such instability is typically due to stage motors, unbalanced thermal chucks, etc. Since the capacitance-time characteristic is strongly temperature-dependent, a known and stable capacitor temperature is essential. The chuck temperature should vary by no more than 1°C during the measurement.

3.2.2 *Light Leaks* — High-quality MOS capacitors are extremely sensitive to low-level light (as their use in CCD imagers attests). Every conceivable source of light must be eliminated. This includes light from hinges, clear plastic vacuum lines, door edges, etc. Light leakage causes the calculated generation velocity to be increased due to electron-hole pair formation by the action of the light.

3.3 *MOS Capacitor Structure Related Errors* — Typical errors due to the MOS capacitor structure include the following sources:

3.3.1 *Lateral-Oxide-Surface-Charge-Spreading (LOS-CS)*¹ — LOS-CS is typically observed in thin silicon dioxide (1000 Å or less) MOS capacitors formed by shadow-masking of the metal gate. Adsorbed water molecules on the oxide surface allow dissociation of surface impurities into ionic forms that respond to the applied gate bias, causing the oxide surrounding the metal dot to become charged. Such response is much slower than the applied oscillator voltage, thereby causing no additional contribution to the measured gate capacitance in accumulation or depletion. In inversion, however, the charged oxide can invert the silicon beyond the gate area. This extended inversion layer can then act as a source for minority carriers, causing the inversion layer under the gate to respond to the oscillator voltage. Such response causes the measured capacitance to increase as the LOS-CS affects the oxide surface charge, causing gross errors in the measured capacitance-time characteristic. LOS-CS results in artificially low values of generation lifetime and high values of generation velocity. Since the charge induced by LOS-CS dissipates very slowly (on the

¹ Nicollian, E. H., and Brews, J. R., *MOS (Metal Oxide Semiconductor) Physics and Technology*, Wiley-Interscience (1982): pp. 148–156.

order of days), LOSCS causes progressive deterioration of capacitance-time characteristics. LOSCS can be avoided by using a guard ring MOS capacitor (refer to Figure 1). The guard ring is biased into accumulation at a voltage sufficient to prohibit LOSCS from affecting the inversion characteristics.

3.3.2 Excessive Series Dissipation Factor — Most commercial capacitance meters are sensitive to the dissipation factor of the capacitor being measured. The series dissipation factor, D_s , is defined by:

$$D_s = 2\pi f R_s C_s \quad (1)$$

where:

f = measurement frequency, Hz,

R_s = series resistance, Ω , and

C_s = series capacitance, F.

When the dissipation factor exceeds some value specified by the capacitance meter manufacturer (usually 0.05 to 0.1), the capacitance measurement accuracy is significantly affected. High series dissipation factor can be caused by poor back surface contact; high resistivity bulk silicon wafers; excessively large capacitors; and/or excessively high measurement frequency.

3.3.3 Processing Contamination — This Test Method requires thermal oxidation of the test wafer to form the MOS structure. In cases where the generation lifetime and generation velocity are being measured to determine the quality of outgoing or incoming silicon wafers, the utmost care must be taken to ensure that the fabrication of the MOS capacitor does not contaminate the test wafer with deep-level impurities, such as transition metals (refer to ¶ 1.1 and Note 1). Sources of contamination include any pre-oxidation cleans, processing gases or chemicals, and furnace quartz ware.

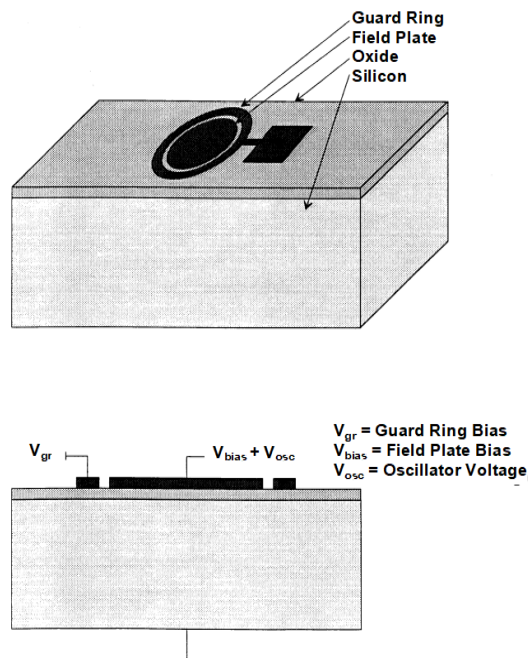


Figure 1
Guard Ring Capacitor Diagrams

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI M59 — Terminology for Silicon Technology

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Terms relating to silicon and other semiconductor technology are defined in SEMI M59.

6 Summary of Test Method

6.1 The small-signal high-frequency capacitance of an MOS capacitor is measured as a function of time, after the capacitor has been subjected to a voltage step from accumulation to inversion. The generation lifetime and generation velocity are determined from an analysis of the capacitance-time data.

6.2 The following assumptions are made in the analysis of the capacitance-time data to determine the generation lifetime and generation velocity:

6.2.1 The majority carrier density is zero within the depletion region and equal to the dopant density outside; the transition at the edge of the depletion region is a step function (depletion approximation).

6.2.2 The voltage drop across the inversion layer is zero.

6.2.3 The dopant density of the silicon wafer (or epitaxial layer) is known and is constant throughout the wafer (or layer).

6.2.4 The relative dielectric constants of the silicon and silicon dioxide are known and constant throughout the materials.

7 Apparatus

7.1 *Facilities for Fabricating the MOS Capacitor* — As customarily used in the facility performing the test.

NOTE 2: Related Information 1 describes a process flow and structure that has been found to be suitable.

7.2 *Digital Capacitance Bridge or Meter* — Capable of measurements from 1 pF to 1000 pF, or greater, full scale. The instrument shall have on each range an accuracy of 1.0% of full scale or better and a reproducibility of 0.25% of full scale or better. The small signal oscillator shall be adjustable to or fixed at a level of 0.010 VAC to 0.050 VAC at a fixed or adjustable frequency in the range from 10 kHz to 1 MHz. The instrument shall supply or allow the application of direct current (dc) bias over the range of ± 100 Vdc (refer to ¶ 7.4). The instrument shall provide data to and be externally controllable by computer.

7.3 *Digital Voltmeter* — With ranges of 1 V to 100 V full scale, a resolution of 0.1% of full scale or better, an accuracy per range of 0.5% of full scale or better, reproducibility of 0.25% of full scale or better, input impedance of 100 M Ω or greater, and a common-mode rejection greater than 100 dB at 60 Hz. The instrument shall provide data to and be externally controllable by computer.

7.4 *Digital DC Power Supply (Two)* — Capable of applying a step change in bias between any two voltages in the range of ± 100 V (open circuit) with a setting resolution of 10 mV or better and ripple of 0.5% of the dc output, or less. One of the supplies may be an integral part of the capacitance bridge or meter (refer to ¶ 7.2). The instruments shall provide data to and be externally controllable by computer.

7.5 *Standard Capacitors (Two)* — Accurate to 0.25% or better at the measurement frequency (refer to ¶ 7.2). One capacitor shall be in the range from 1 pF to 10 pF, inclusive and one shall be in the range from 10 pF to 100 pF, inclusive. The two capacitor values should differ by at least a factor of 10.

7.6 *Precision DC Voltage Source* — Capable of providing output voltages from 0 V to ± 100 V with an accuracy of 0.1% of the output voltage or better.

7.7 *Thermometer (Digital or Analog) or Thermocouple* — With a range of 0°C to 100°C and an accuracy of 0.5°C or better, to be attached to the metal chuck (refer to ¶ 7.8).

7.8 *Probe Fixture and Enclosure* — The fixture shall hold the test wafer and provide the following: probes for making contact to the gate and the guard ring, a metal chuck for back surface contact, vacuum clamping of the test wafer to the chuck, and a means for attaching a thermometer or thermocouple to the chuck (refer to Figure 2). The enclosure