

SEMI MF154-1105 (Reapproved 0611) GUIDE FOR IDENTIFICATION OF STRUCTURES AND CONTAMINANTS SEEN ON SPECULAR SILICON SURFACES

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NOTICE: This document was reapproved with minor editorial changes.

1 Purpose

- 1.1 The purpose of this guide is to list, illustrate, and provide reference for various characteristic features and contaminants that are seen on highly specular silicon wafers.
- 1.2 Ambiguities and uncertainties regarding surface defects may be resolved by reference to this guide.
- 1.3 There is close alignment between this guide and common specifications used for the purchase of silicon wafers.

2 Scope

- 2.1 This guide contains a compilation of the most commonly observed singularly discernible structures on specular silicon surfaces.
- 2.2 Recommended practices for delineation and observation of these artifacts are referenced. The artifacts described in this guide are intended to parallel and support the content of the specification form for order entry in SEMI M1, SEMI M57, and other silicon wafer specifications.
- 2.3 These artifacts and common synonyms are arranged alphabetically in Table 1 and Table 2, and illustrated in Figure 1 through Figure 79.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

- 3.1 Defects, structures, features, or artifacts revealed or enhanced by the referenced methods and exhibited in this guide must be carefully interpreted. Unless utmost care is exercised, the identification of the structure may be ambiguous.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M57 — Guide for Specifying Silicon Annealed Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF1725 — Guide for Analysis of Crystallographic Perfection of Silicon Ingots

SEMI MF1726 — Guide for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

Table 1 Wafer Structural Defects^{#1, #2, #3}

<i>Defect</i>	<i>Common Synonyms and Acronyms</i>	<i>Illustrating Figure(s)</i>	<i>Relevant Standard(s)</i>
Dislocation etch pit	etch pit, pit	1-5	SEMI MF1725
Epitaxial stacking fault	epi stacking fault, (ESF) Epitaxial growth hillock	6-21	SEMI MF1726 SEMI M35
Lineage	Grain Boundary	22	SEMI MF1725
Oxidation induced stacking fault	oxidation stacking fault, (OSF), oxidation induced stacking fault (OISF)	23-29	SEMI MF1727 SEMI MF1809
Oxide precipitates	bulk micro-defect, (BMD), bulk precipitate	30	SEMI MF1727 SEMI MF1809
Shallow pits	S-pit, saucer pit	31-32	SEMI MF1727 SEMI MF1809
Slip	slip lines	33-36	SEMI MF1725 SEMI MF1727 SEMI MF1809
Swirl		37-38	SEMI MF1725 SEMI MF1727 SEMI MF1809
Twin	twin lamella, twin line	39-41	SEMI MF1725

#1 Magnifications given in the attached illustrations are for an original frame size of 50 mm × 50 mm, except as noted.

#2 Unless otherwise noted, all attached figures illustrate polished silicon wafer surfaces.

#3 Unless otherwise noted, all attached figures with magnified images were created using interference contrast microscope equipment.

Table 2 Polished Surface Visual Characteristics

<i>Defect</i>	<i>Common Synonyms and Acronyms</i>	<i>Illustrating Figure(s)</i>	<i>Relevant Standard</i>
Area contamination	Contamination, foreign matter, residue	42-43	SEMI MF523 SEMI M35
Crack	Cleavage, fracture	44-49	SEMI MF523
Crater	Slurry ring	50	SEMI MF523
Crow's feet	Contact damage	51	SEMI MF523
Dimple	Depression	52-53	SEMI MF523
Dopant striation ring	Striation	54	SEMI MF523
Edge chip	Chip	55-58	SEMI MF523
Edge crack	Crack	59	SEMI MF523
Edge crown		60	SEMI MF523
Epitaxial large point defect	large light point defect, (LLPD), spike	61	SEMI MF523
Foreign matter	Contamination, residue	62-63	SEMI MF523
Groove	Polished over scratch, microscratch	64-65	SEMI MF523
Haze		66-67	SEMI MF523 SEMI M35
Localized light scatterers (particle contamination)	large light scatterers, (LLS)	68-69	SEMI MF523 SEMI M35

<i>Defect</i>	<i>Common Synonyms and Acronyms</i>	<i>Illustrating Figure(s)</i>	<i>Relevant Standard</i>
Mound		70	SEMI MF523 SEMI M35
Orange peel	Roughness	71	SEMI MF523
Pits	Air pocket, hole, crystal originated pit, (COP) insufficient polish	72-74	SEMI MF523 SEMI M35
Saw mark		75	SEMI MF523
Scratches	Handling damage	76-78	SEMI MF523
Stain		79	SEMI MF523

5 Terminology

5.1 Terms related to silicon technology, including the features and contaminants discussed in this guide, are defined in SEMI M59.

6 Procedure

6.1 Procedures for visually examining silicon wafers for the features and contaminants discussed in this guide are covered in SEMI MF523, SEMI MF1725, SEMI MF1726, SEMI MF1727, SEMI MF1809, and SEMI MF1810.

6.2 Issues related to examining some of these features and contaminants by scanning surface inspection systems are discussed in SEMI M35.

7 Keywords

7.1 contaminant; defects; dislocation; epitaxial; fracture; preferential etch; scratch; shallow pit; silicon; slip; stacking fault

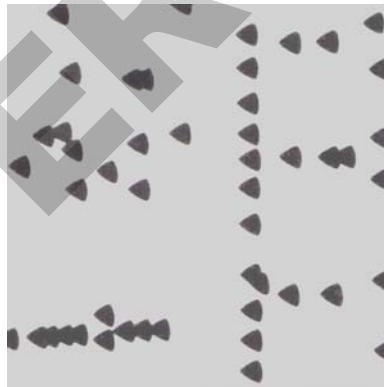


Figure 1
Dislocation Etch Pits on (111) Silicon, Following 3-Min Sirtl Etch,
Magnification 110×



Figure 2
Dislocation Etch Pits on (110) Silicon, Following 5-Min Wright Etch,
Magnification 110×

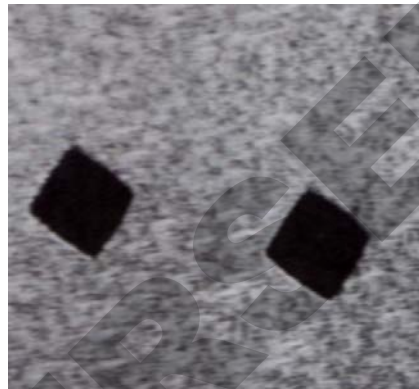


Figure 3
Dislocation Etch Pits on (100) Silicon, Following Schimmel (B) Preferential Etch,
Magnification 320×

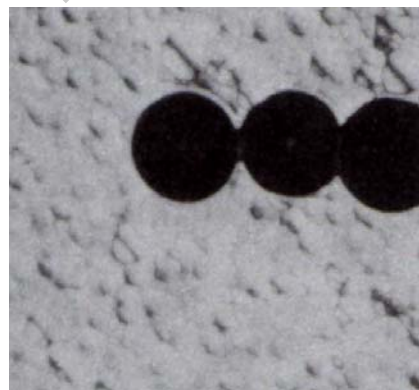


Figure 4
Dislocation Etch Pits on (100) Silicon Following Sirtl Etch,
Magnification 400×

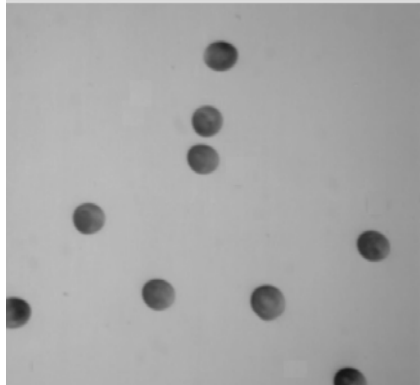


Figure 5
Dislocation Etch Pits on (100) Silicon Following 5-Min Wright Etch,
Magnification 200×

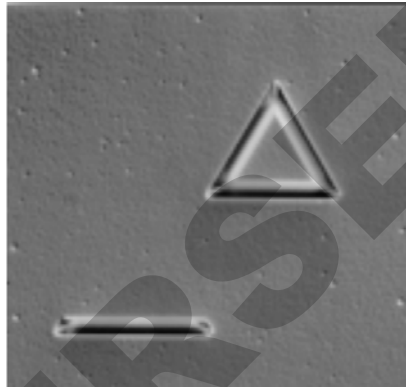


Figure 6
Epitaxial Stacking Faults on (111) Following 4.2 m Dash etch,
Size Dependent Upon EPI Thickness

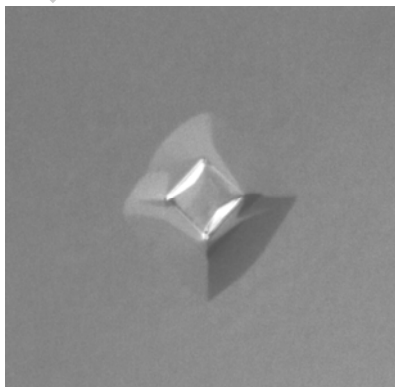


Figure 7
Epitaxial Stacking Faults on (100), No Preparation Required,
Size Dependent Upon EPI Thickness

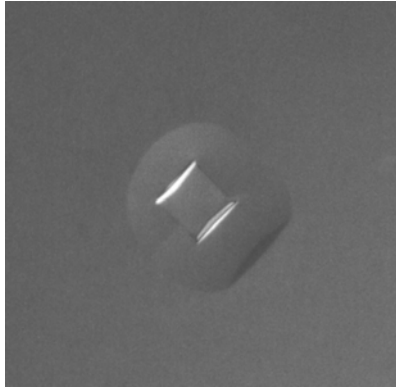


Figure 8
Epitaxial Stacking Faults on (100), No Preparation Required,
Size Dependent Upon EPI Thickness



Figure 9
Epitaxial Growth Hillock on (100), No Preparation Required,
Size Dependent Upon EPI Thickness

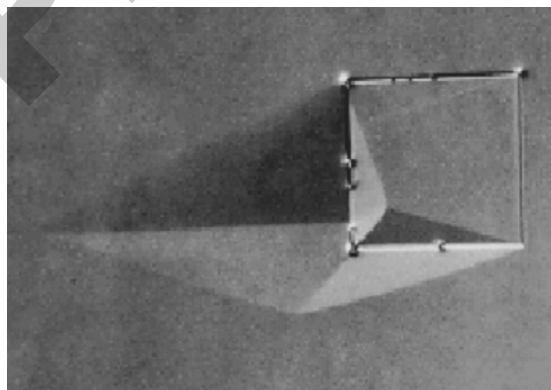
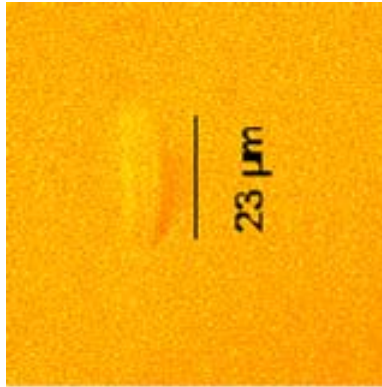
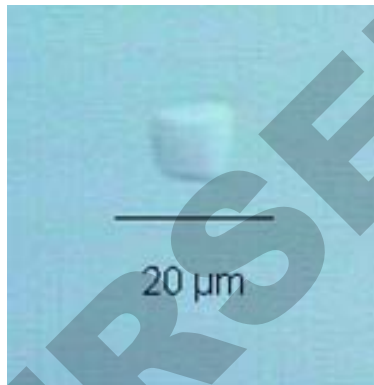


Figure 10
Epitaxial Stacking Faults on (100), No Preparation Required,
Size Dependent Upon EPI Thickness



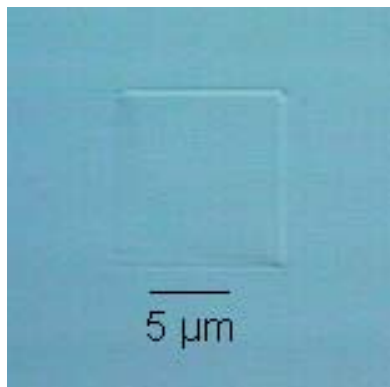
NOTE: Approximate SSIS scattering event size: 0.22 μm .

Figure 11
Epi Growth Hillock



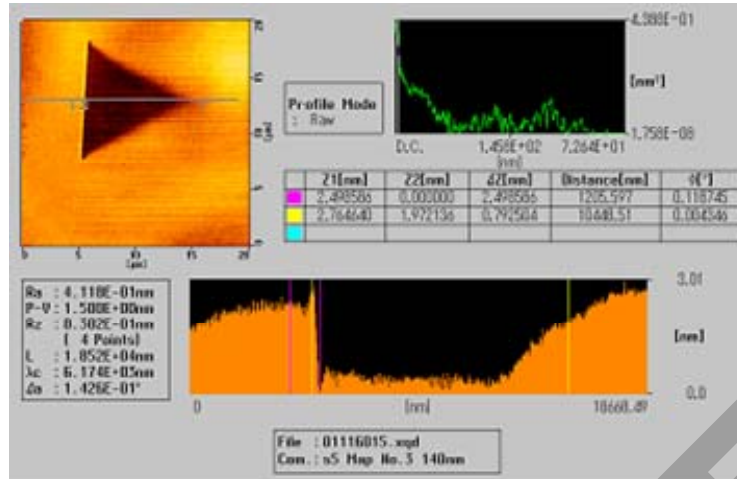
NOTE: Approximate SSIS scattering event size: 0.15 μm .

Figure 12
Epi Growth Hillock



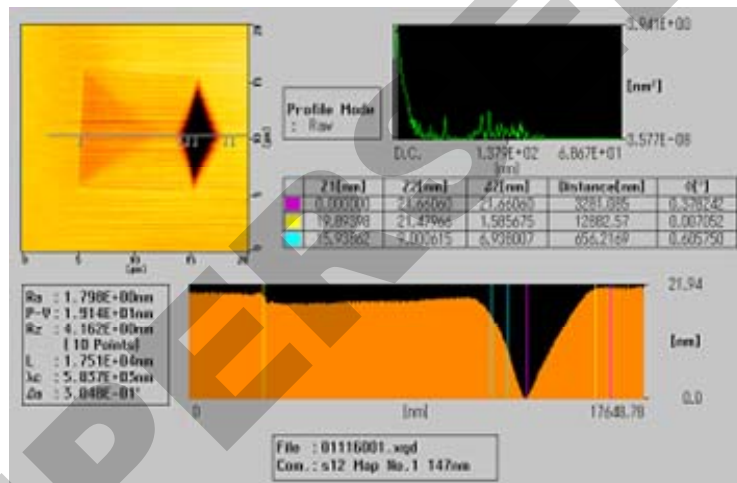
NOTE: Approximate SSIS scattering event size: 0.165 μm .

Figure 13
Epitaxial Stacking Fault



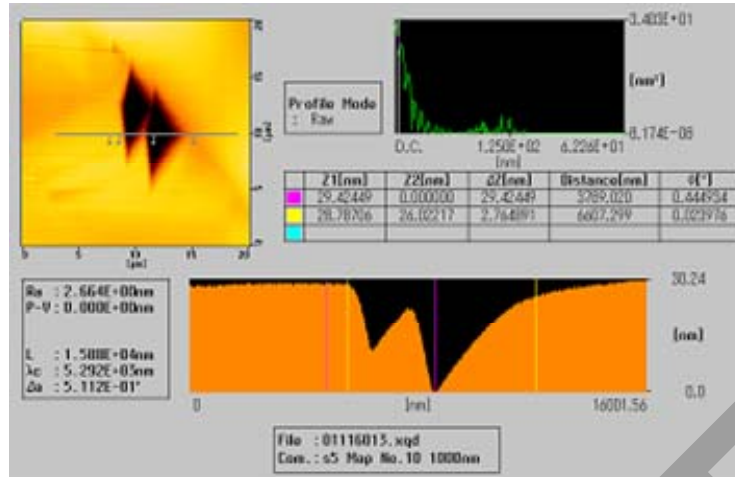
NOTE: Approximate SSIS scattering event size: 0.12 μm .

Figure 14
Atomic Force Microscope (AFM) Image of Epitaxial Stacking Fault



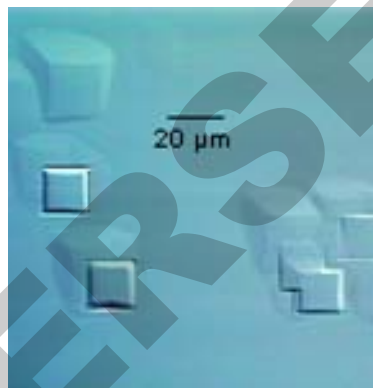
NOTE: Approximate SSIS scattering event size: 0.30 μm .

Figure 15
AFM Image of Epitaxial Stacking Fault Showing Four Sides and Deep Depression of ~20 nm on One Side



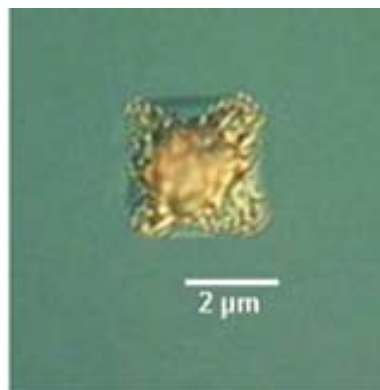
NOTE: Approximate SSIS event scattering size: 1.05 μm

Figure 16
AFM Image of Double Epitaxial Stacking Fault



NOTE: Approximate SSIS scattering event size: 0.20 μm

Figure 17
Epitaxial Stacking Fault Cluster



NOTE: Approximate SSIS scattering event size: $>>1.0 \mu\text{m}$

Figure 18
Composite Defect of Polysilicon Growth and Stacking Faults