

SEMI MF1726-1110 (Reapproved 0322) PRACTICE FOR ANALYSIS OF CRYSTALLOGRAPHIC PERFECTION OF SILICON WAFERS

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NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

1.1 The use of silicon crystals in many semiconductor devices requires a consistent atomic lattice structure. Crystal defects disturb local lattice energy conditions that are the basis for semiconductor behavior. These defects have distinct effects on essential semiconductor-device manufacturing processes such as alloying and diffusion.

1.2 Epitaxial growth processes are used extensively in the manufacture of silicon electronic devices. Stacking faults introduced during epitaxial growth can cause ‘soft’ electrical characteristics and preferential micro plasma breakdowns in diodes.

1.3 Epitaxial defects are more clearly delineated with the use of this destructive etching procedure. Epitaxial wafers may however be classified nondestructively by this method without the destructive preferential etching and inspection steps.

1.4 This Practice provides guidance regarding procedures for analysis of crystal defects of silicon ingots from which silicon wafers are cut.

1.5 This Practice, together with the referenced standards, may be used for process control, research and development, and material acceptance purposes.

2 Scope

2.1 This Practice covers the determination of the density of crystallographic defects in unpatterned polished and epitaxial silicon wafers. Epitaxial silicon wafers may exhibit dislocations, hillocks, shallow pits or epitaxial stacking faults, while polished wafers may exhibit several forms of crystallographic defects or surface damage. Use of this Practice is based upon the application of several referenced standards in a prescribed sequence to reveal and count microscopic defects or structures.

2.2 This Practice is suitable for use with epitaxial or polished wafers grown in either [111] or [100] direction and doped either *p*- or *n*-type with resistivity greater than 0.005 $\Omega \cdot \text{cm}$.

2.3 This Practice is suitable for use with epitaxial wafers with layer thickness greater than 0.5 μm .

2.4 Additional requirements on the material to be tested are listed in SEMI MF1810.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M59 — Terminology for Silicon Technology

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafers Surfaces

SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers

3.2 ISO Standards¹

ISO 14644-1 — Cleanrooms and Associated Controlled Environments – Part 1: Classification of Airborne Particulates

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Acronyms, terms, and symbols related to silicon technology, including those used in these practices, are listed and defined in SEMI M59.

5 Summary of Practice

5.1 Clean, unprocessed polished or epitaxial wafers are selected. The wafers are examined under bright light illumination to ensure that they are free from contamination and obvious surface damage. Epitaxial wafers may also be microscopically inspected before etching to count and classify visible imperfections. Wafers are then etched in a preferential defect etchant solution. The etched surface is again examined under bright light illumination to identify patterns that may be related to contamination or improper handling. The imperfections highlighted by the preferential etchant are then microscopically counted and classified.

6 Apparatus

6.1 *Safety Equipment and Facility* — For defect etching as described in SEMI MF1809.

6.2 *Wafer Inspection Facilities and Handling Equipment* — Consistent with industry practice and suitable for use with SEMI MF523.

7 Reagents and Materials

7.1 Refer to SEMI MF1809 for specific information on reagents and materials.

8 Procedure

8.1 Select an unprocessed, polished or epitaxial wafer, ready for use in the fabrication of electronic devices.

8.1.1 Open the wafer container in a particle-controlled environment of class 6 or better as indicated in ISO 1466-1 to prevent introduction of additional defects.

8.1.2 Transfer the wafer with a robotic tool or a nonmetallic vacuum pencil, contacting the wafer edge or back surface. Ensure that the front surface of the adjacent wafer is not contacted during the removal.

NOTE 1: Any contact with the front surface of the adjacent wafer can transfer contamination and generally scratch the surface.

8.2 Preliminary Sample Inspection

8.2.1 Inspect the first sample using high intensity light conditions as described in SEMI MF523 to identify any surface imperfections, scratches, or contamination hazes that may interfere with the etching process or confound the result. If any of these interferences are detected, select a separate sample for analysis.

NOTE 2: These interferences can generate artifacts that may be confused with the true defects.

8.2.2 *Epitaxial Wafer, Nondestructive Defect Counting* — Inspect epitaxial wafers microscopically in accordance with SEMI MF1810 before defect etching to count most of the epitaxial stacking fault defects.

¹ International Organization for Standardization, ISO Central Secretariat, BIBC II, Chemin de Blandonnet 8, CP 401, 1214 Vernier, Geneva, Switzerland; Telephone: +41.22.749.01.11, <http://www.iso.org>