

SEMI MF1727-1110 (Reapproved 1115) PRACTICE FOR DETECTION OF OXIDATION INDUCED DEFECTS IN POLISHED SILICON WAFERS

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NOTICE: This Document was reapproved with minor editorial changes.

1 Purpose

- 1.1 Defects induced by thermal processing of silicon wafers may adversely influence device performance and yield.
- 1.2 These defects are influenced directly by contamination, ambient atmosphere, temperature, time at temperature, and rate of change of temperature to which the specimens are subjected. Conditions vary significantly among device manufacturing technologies. The thermal cycling procedures of this Practice are intended to simulate basic device processing technologies. Oxidation cycles other than specified herein, or multiple oxidation cycles, may sometimes more accurately simulate device-processing procedures. The results obtained may differ significantly from those obtained with the specified oxidation cycles.
- 1.3 The geometry of some patterns revealed by this Practice suggests that they are related to the crystal growth process while others seem related to surface preparation or thermal cycling conditions.
- 1.4 This Practice is suitable for acceptance testing when used with referenced practices and methods.

2 Scope

- 2.1 This Practice covers the detection of crystalline defects in the surface region of silicon wafers. The defects are induced or enhanced by oxidation cycles encountered in normal device processing. An atmospheric pressure oxidation cycle representative of bipolar, metal-oxide-silicon (MOS) and CMOS technologies is included. This Practice reveals strain fields arising from the presence of precipitates, oxidation induced stacking faults, and shallow etch pits. Slip is also revealed that arises when internal or edge stresses are applied to the wafer.
- 2.2 Application of this Practice is limited to specimens that have been chemical or chemical/mechanical polished to remove surface damage from at least one side of the specimen. This Practice may also be applied to detection of defects in epitaxial layers.
- 2.3 The surface of the specimen opposite the surface to be investigated may be damaged deliberately or otherwise treated for gettering purposes or chemically etched to remove damage.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

- 3.1 Material having residual work damage in the polished surface exhibits visible patterns when the procedures of this Practice are used. Usually, edge damage, lapping damage, tool marks, or scratches are easily identified by the location and pattern observed.
- 3.2 Contamination not removed by preparatory cleaning procedures or deposited following cleaning, may become visible after oxidation and preferential etching.
- 3.3 Slip may be introduced by differential expansion at the points of wafer support in the furnace boat. Slip radiating from the points of support may be assumed to originate from this boat pinch and not be inherent in the unprocessed wafer. Slip may also be caused by large thermal gradients imposed across a wafer by fast insertion or removal from the furnace.
- 3.4 If the oxidation furnace or apparatus is contaminated, it can cause extraneous artifacts or defects.

3.5 Striations, helical features on the surface of a silicon wafer, are ascribed to periodic dopant incorporation differences occurring at the rotating solid-liquid interface during crystal growth. These features are visible to the unaided eye after preferential etching, seem continuous under 100× magnification, and may be confused with ring patterns of oxidation stacking faults.

3.6 Otherwise identical wafers with different back surface conditions may yield different results by this Practice.

3.7 Wafers, particularly <111> orientation, may show lower shallow-pit defect density when the back surface of the wafer is gettered. Backside gettering should be noted in the sample classification when data are reported.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI C28 — Specifications for Hydrofluoric Acid

SEMI C54 — Specifications and Guidelines for Oxygen

SEMI C58 — Specifications for Hydrogen

SEMI M59 — Terminology of Silicon Technology

SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers

4.2 ASTM Standard¹

ASTM D5127 — Standard Guide for Ultra-Pure Water Used in the Electronics and Semiconductor Industries

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Acronyms, terms, and symbols related to silicon technology, including those used in this Practice, are listed and defined in SEMI M59.

6 Summary of Practice

6.1 Wet oxidation is used to generate or highlight defects, or both, in silicon wafers. This oxidation may also simulate simple device production processes.

6.2 The defects are revealed subsequently by preferential etching and examination by interference contrast microscopy according to referenced SEMI Standards.

7 Apparatus

7.1 *Oxidation Furnace* — Furnace shall be consistent with the intended process application and shall sustain a designated temperature with uniformity less than $\pm 5^{\circ}\text{C}$ over a zone at least 0.3 m long.

7.2 *Steam Source* — Wet oxidation shall be carried out using a pyrogenic steam generator to provide steam.

7.3 *Working Chamber* — A pure, fused quartz, silicon carbide, or silicon tube of an inside diameter sufficient to hold the specimen wafers. The inlet end shall be fitted with the appropriate pyrogenic torch apparatus. The exhaust end shall be fitted to exhaust the process gases to satisfy applicable environmental requirements and prevent back streaming of outside air into the working chamber.

7.4 *Wafer Boat* — A quartz, silicon or silicon carbide fixture for holding the specimen wafers either parallel or perpendicular to the gas flow in the furnace.

7.5 *Pickup Tool* — A manual or automated transfer tool fitted with a nonmetallic material such as quartz or TFE-fluorocarbon. The pickup tool shall be constructed so that no metal can contact the specimen wafer.

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