

SEMI MF1771-0416 (Reapproved 1121) TEST METHOD FOR EVALUATING GATE OXIDE INTEGRITY BY VOLTAGE RAMP TECHNIQUE

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NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and §§) the symbols are used to reference more than one section or paragraph, respectively.

1 Purpose

1.1 The technique outlined in this Test Method is meant to standardize the procedure, analysis and reporting of oxide integrity data via the voltage ramp technique among interested parties. However, since the values obtained cannot be entirely divorced from the process of fabricating the test structure, suitable correlations should be performed based on process needs and structure selection. This correlation should include sample size as well as device geometry.

1.2 Measurement of the electrical integrity of oxides grown on silicon wafers may also be used in-house as a means of monitoring the quality of furnaces and other processing steps as well as judging the impact of changing some processing steps.

1.3 Selection of various edge and area intensive structures is crucial for isolating the nature of the defects. Techniques for using such structures to isolate the nature of detected defects is beyond the scope of this Test Method.

1.4 The actual results are somewhat dependent on the choice of gate electrode. Polysilicon gates have the advantage of being identical to finished product in many instances. Even for polysilicon gates, exact results depend upon values chosen for polysilicon thickness, doping, and sheet resistance.

2 Scope

2.1 The techniques outlined in this Standard are for the purpose of standardizing the procedure of measurement, analysis, and reporting of oxide integrity data between interested parties.

2.1.1 This Test Method makes no representation regarding actual device failure rates or acceptance/rejection criteria.

2.1.2 While some suggestions for data analysis are included in later sections of this Test Method, interpretation of results is beyond the scope of this Standard. Any such interpretations should be agreed upon between interested parties prior to testing. For example, a variety of failure criteria are included to permit separation of so-called intrinsic and extrinsic oxide failures.

NOTE 1: In this regard this Test Method differs from that given in SEMI M51, which is focused on application of gate oxide integrity measurements, as described in this Test Method, to determine the density of crystal originated pits in the wafer under test. SEMI M51 also provides a standardized procedure for fabricating the MOS capacitors.

2.2 The background of this Test Method is provided in Related Information 1.

2.3 This Test Method covers the procedure for gauging the electrical strength of silicon dioxide thin films with thicknesses ranging from approximately 3 to 50 nm. In the analysis of films of 4 nm or less, the impact of direct tunneling on the current-voltage characteristics, and hence the specified failure criteria defined in § 2.5, must be taken into account. Since oxide integrity strongly depends on wafer defects, contamination, cleanliness, as well as processing, the users of this Test Method are expected to include wafer manufacturers and device manufacturers.

2.4 This Test Method is not structure specific, but notes regarding options for different structures may be found in Related Information 2. The three most likely structures are simple planar metal-oxide semiconductor (MOS-

capacitors) (fabricated or mercury probe), various isolation structures (e.g., local oxidation of silicon [LOCOS]), and field effect transistors. This Test Method assumes that a low resistance ohmic contact is made to the backside of each wafer in each case. For a more detailed discussion of the design and evaluation of test structures for this Test Method, the reader is referred to the JESD 35-1.

2.5 Failure criteria specified in this Test Method include both the fixed current limit (soft) and destructive (hard) types. In the past, use of a fixed current limit of 1 μA or more virtually ensured measurement of hard failure, as the thicker, more heavily contaminated oxides of those days typically failed catastrophically as soon as measurable currents were passed. The cleaner processing of thinner oxides now means that oxides will sustain relatively large currents with little or no evidence of failure. While use of fixed current limit testing may still be of value for assessing uniformity issues, it is widely felt that failure to continue oxide breakdown testing to the point of catastrophic oxide failure may mask the presence of defect tails, which are of critical importance in assessing long-term oxide reliability. For this reason, this Test Method makes provision for use of fixed limit failure criteria if desired and agreed upon by the parties to the testing, but specifies that testing be continued until hard failure is sensed.

2.6 This Test Method specifically does not include measurement of a charge-to-breakdown (Q_{bd}) parameter. Industry experience with this parameter measured in a ramp-to-failure test such as this indicates that Q_{bd} values so obtained may be unreliable indicators of oxide quality. This is because a large fraction of the value determined is collected in the last steps of the test, and the result is subject to large deviations. Q_{bd} should be measured in a constant current or bounded current ramp test. This Test Method is applicable to both n -type and p -type wafers, polished or having an epitaxial layer. In wafers with epitaxial layers, the conductivity type of the layer should be the same as that of the bulk wafer. While not excluding depletion polarity, it is preferred that measurement polarity should be in accumulation to void the complication of a voltage drop across the depletion layer.

2.7 While this Test Method is primarily intended for use in characterizing the SiO_2 -silicon systems as stated above, it may be applied in general terms to the measurement of other metal-insulator-semiconductor structures if appropriate consideration of the characteristics of the other materials is made.

2.8 Measurement conditions specified in this Test Method are conservative, intended for thorough analysis of high quality oxide-silicon systems, and to provide a regime in which new users may safely begin testing without encountering undue experimental artifacts. It is recognized that some experienced users may be working in applications where less precise data is required and a more rapid test is desirable. An example of this situation is the evaluation of silicon wafer quality, where a staircase voltage step providing 0.5 MV/cm oxide field strength resolution and a voltage step duration of 0.2 s has been used. Such test conditions may be specified when agreed upon as adequate by all participants to the testing. Because the dependence of measured parameters upon test conditions may increase as these conditions depart from those specified in this Test Method, it is important that all parties to these tests use the same set of test conditions, so that their results are comparable.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Since this is a DC measurement, care must be taken to make sure that the wafer has a low resistance ohmic return contact. This is preferably done with a metallized contact to the back side of the wafer under test. In cases where testing must be done on capacitors in diffused wells of conductivity type opposite to the substrate, top side contacts carefully designed to provide uniform, low resistance to all parts of the test capacitor should be used. A discussion of these design criteria is given in JESD 35-1.

3.2 It is strongly suggested that testing be done with a voltage polarity to accumulate the silicon surface underlying the oxide; positive voltages for n -type substrates and negative voltages for p -type substrates. If this is not done, a topside contact to a diffused region of opposite conductivity type surrounding the capacitor (a gated diode or transistor) should be used to minimize the problem of uncontrolled voltage drops across the inversion layer during testing. This is an absolute requirement for testing p -type substrate capacitors under positive bias, where sufficient electrons to support conduction and breakdown are not available without the n -type region.

3.3 Evaluation and control of electrical noise in the current-voltage data taken as part of this Test Method is crucial to the proper identification of the failure criteria, particularly the $\ln J$ -V slope change criterion defined in ¶ 9.9.4. Approaches for minimizing electrical noise in the measurements are suggested in § 7 on Apparatus, and an approach for noise evaluation is given in ¶ 10.3.

3.4 Control of the voltage step time may be difficult when using automated electrometers in a voltage staircase regime. While the required 100 ms step time may be set using a delay in the measurement loop, an additional, uncontrolled delay may be incurred due to auto-ranging of the electrometer. The effect is most pronounced for very low currents, where the measured value is several orders of magnitude below the minimum range set by the electrometer software. An example of this effect is discussed in ¶ 10.3.

3.5 The method of probing the device may affect the results. Examples of possible variables are probe pressure and use of a contact pad versus direct contact to the gate.

3.6 Use of gate electrode material other than polysilicon may mask differences in materials and make the material look worse than it might otherwise appear if polysilicon gates are used. This is because the process of forming a gate electrode on an oxide sample may affect the integrity of that oxide either for better or for worse. Sputtering or radiation damage accompanying metal gate deposition may degrade oxide integrity, while the high temperature annealing and gettering associated with polysilicon deposition and doping may improve oxide quality. On the other hand, stress arising from crystal formation in the polysilicon, or impurity diffusion along polysilicon grain boundaries may degrade oxide integrity. Changes of gate-substrate work function difference may also affect the breakdown and wearout mechanisms in the oxide. Therefore, potential effects of gate electrode material choice on test results must not be neglected.

3.7 The actual values obtained depend somewhat on the processing involved in fabricating the test structure. Care must be taken to ensure a consistent processing.

3.8 Wafer temperature during testing should be clearly defined. While oxide breakdown voltages are not strongly temperature-dependent, the oxide wearout mechanism is temperature-sensitive, and large temperature variations might have an impact on results.

3.9 **WARNING:** Since the voltage and currents involved are potentially dangerous, appropriate means of preventing the operator from coming into contact with the probe tip or other charged surfaces should be in place before testing.

3.10 When testing very thin oxides, those 10 nm or less in thickness, special care must be taken to account for effects arising from the very high specific capacitance of these films. These may include voltage drops across the polysilicon gate electrode and the silicon substrate, and high conduction due to direct tunneling.

3.11 When using a mercury probe for measurements of this type, care must be taken in the preparation and control of the oxide surface. Adsorbed organic contaminant films may affect the electric field distribution in the oxide. Such films may sometimes be removed with hot SC-1 cleaning solution; a mixture of NH_4OH - H_2O_2 - H_2O . Use of a dry nitrogen purge of the probing ambient is also recommended to minimize surface contamination effects.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI M51 — Test Method for Characterizing Silicon Wafers by Gate Oxide Integrity

SEMI M59 — Terminology for Silicon Technology

4.2 JEDEC Standards¹

JESD 35A — Procedure for the Wafer-Level Testing of Thin Dielectrics

JESD 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

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5 Terminology

5.1 Acronyms, terms, and symbols related to silicon technology, including those used in this Test Method, are listed and defined in SEMI M59.

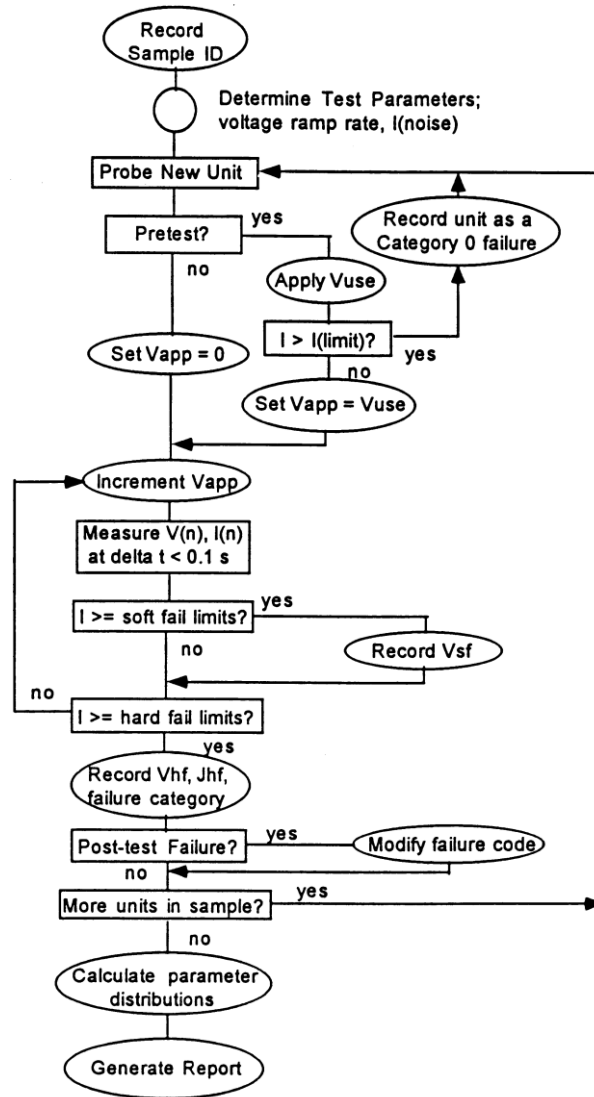


Figure 1
Flow Diagram for Ramp Voltage Test Method

5.1.1 These categories have traditionally been used for oxides thicker than about 20 nm. For thinner films, care must be taken in their use and in proper derivation of the oxide field strengths as described in ¶ 10.2. The break point between A mode and B mode failure in this set of categories is different from the 3 MV/cm given in SEMI M51.

6 Summary of Test Method

6.1 A flow diagram for the ramp voltage test is pictured in Figure 1.

6.2 Record the test specimen ID and other test identity.

6.3 Establish the test parameters relevant to the test system and to the test specimen.

6.4 A capacitor unit on the test specimen is selected for test, and an optional pretest of capacitor leakage is carried out, if desired.

6.5 If the capacitor fails this pretest, the capacitor is recorded as a category 0 failure and a new capacitor on the test specimen is selected for test.

6.6 Otherwise, the voltage on the capacitor is set to 0 (if no pretest was conducted) or to the voltage of use (if a pretest was carried out).

6.7 The voltage applied to the capacitor under test is increased linearly with time at a specified rate, with measurements of current made at intervals that must correspond to oxide electric field changes less than a maximum specified value.

6.8 The voltage ramp continues until hard failure (destructive breakdown), as defined by one of several specified failure criteria, is sensed and stored along with the appropriate hard failure criterion.

NOTE 2: In this Test Method, hard failure is sensed by an abrupt, irreversible change in the current-voltage characteristics of the capacitor, for example by a relatively large change in dc conduction level between voltage steps or as a change in the logarithmic slope of the current density-voltage characteristic.

6.9 During the measurement cycle, soft failures corresponding to predetermined current levels are sensed and stored.

NOTE 3: Soft failure may be either destructive or nondestructive, as in the case of Fowler-Nordheim or direct tunneling currents.

6.10 The measurement cycle for this capacitor is completed when hard failure is detected or when the upper voltage limit of the test is reached.

6.11 After the test is completed (without observing hard failure), a post-test is performed to evaluate hard failure by sensing current at a low voltage.

6.12 The test cycle is then repeated for the next capacitor in the array, and this is continued until all units in the specified group have been tested.

6.13 When testing is complete, calculations and categorizing of data is done and a report is generated.

7 Apparatus

7.1 Although the Test Method is independent of equipment configuration, the use of computer-controlled probing equipment is essential as the measurement speed precludes manual data gathering. What is included here shall be considered a minimum.

7.1.1 *Voltage Source and Sink* — That is capable of delivering/receiving between 0 and ± 100 V in the form of an effective ramp rate of 1.0 ± 0.1 MV/cm⁻¹/s⁻¹ either automatically or under computer control. If use of other ramp rates is mutually agreed upon (see § 9.6), it must be established that hardware is available to perform the measurement adequately. This voltage source/sink may consist of two source-measurement units (SMU's) with a common ground, or just a single SMU with a dedicated sink. The voltage source shall be capable of sourcing at least 100 mA of current.

7.2 *Shielded Triaxial Cables* — Involving guarding to minimize the noise when measuring low current values.

7.3 *Wafer Chuck* — Electrically isolated from its case/probe platen. While the chuck may be connected to the reference voltage (zero, not ground), lower electrical noise may be obtained by connecting the voltage ramp source to the chuck and measuring the current through the probe connection.

7.4 *Probe* — To contact the gate electrode. Either a hard needle-type probe such as tungsten carbide (which may be a single probe or a probe card) or a mercury probe may be used.

8 Sampling

8.1 Sampling is the responsibility of the user of this Test Method. However, if testing is done as part of a comparison or correlation, sampling shall be agreed upon in advance by all participants.

NOTE 4: Refer to the appendix of JESD 35A for a good discussion of sampling plan statistics.